VocalFusion® XVF3510-UA Voice Processor Datasheet

V4.1

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PRODUCT FEATURES

The VocalFusion® XVF3510-UA is a high-performance voice processor optimised for USB applications with the following features:

VOICE PROCESSING

- Two PDM microphone inputs
- Digital signal processing pipeline
  - Full duplex, stereo, acoustic echo cancellation
  - Reference audio via USB with automatic bulk delay insertion
  - Point noise suppression via an interference canceller.
  - Switchable stationary noise suppressor
- Programmable Automatic Gain Control (AGC)
- Flexible audio output routing and filtering
- Independent audio paths for communications and Automatic Speech Recognition (ASR)

DEVICE INTERFACES

- Full speed USB2.0 compliant device supporting USB Audio Class (UAC) 1.0
- USB HID and Endpoint 0 control interfaces
- Flexible peripheral interfaces
  - Programmable digital general-purpose inputs and outputs
  - I2C master interface for control of local I2C based devices
  - I2S master interface output of audio data, and optional reference input
  - SPI master interface for control and interrogation of a local SPI slave devices

FIRMWARE MANAGEMENT

- Boot from QSPI flash
  - Default firmware image for power-on operation
  - Update image delivered via USB
  - Persistent user data maintained across firmware upgrade cycles
  - Storage of user-defined tuning parameters
  - User-programmable setup of I2C/SPI peripherals
- Option to boot from a local host processor via SPI
- Device firmware update for over-the-air device management

PACKAGE

- 7mm x 7mm 60pin QFN package

POWER CONSUMPTION

- Typical power consumption 500mW during active processing

CONTENTS

1. VOCALFUSION XVF3510-UA VOICE PROCESSOR

1.1. XVF3510-UA OVERVIEW

The XMOS VocalFusion® XVF3510 range of processors use microphone array processing to capture clear, high-quality audio from anywhere in the room. XVF3510 processors use highly optimised digital signal processing algorithms to implement 'barge-in', suppress point noise sources and reduce ambient noise levels increasing the effective Signal to Noise Ratio (SNR) to achieve a reliable voice interface whatever the environment.

The processor is designed for seamless integration into consumer electronic products requiring voice interfaces for Automatic Speech Recognition (ASR), or communication and conferencing. In addition to the class leading voice processing, XVF3510-UA processor implements specific features required for use in USB accessory applications as shown below.

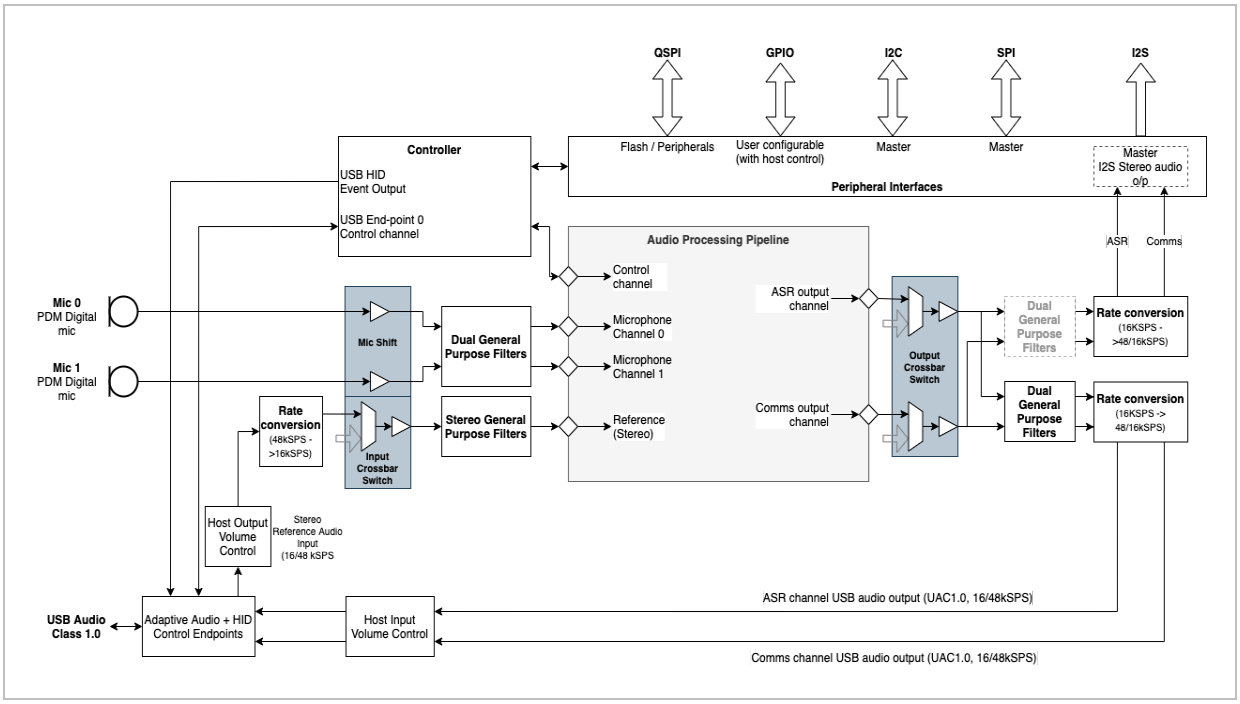


Figure 1-1 Functional block diagram of XVF3510-UA

The VocalFusion XVF3510 voice processor converts and enhances audio captured using a pair of low-cost digital microphones. Processed audio streams are suitable for use in Automatic Speech Recognition (ASR) or voice communications applications and benefit from a range of configurable audio processing techniques to allow customisation to the use case. The included audio processing provides the following features:

- Two microphone far-field operation.
- Full 360-degree operation in “coffee table” applications or 180 degrees for operation in edge-of-room products such as smart TVs.
- 16kHz voice processing, with optional 16kHz and 48kHz interface sample rates.
- Full duplex, stereo, Acoustic Echo Cancellation (AEC) with a maximum tail length of 225ms accommodating the most reverberant environments. (Reference audio for cancellation can be provided via USB or I2S.)
- Automatic bulk delay insertion, of up to 150ms, to account for positive or negative reference audio delays ensuring optimal echo cancellation with all audio output paths.
- Cancellation of point noise sources via a 256 frequency band Interference Canceller.
- Switchable stationary noise suppressor.

- Adjustable gain over a 60dB range with Automatic Gain Control (AGC).
- Audio output filtering and range limiter.
- Independent audio processing paths and control of parameters for communications and ASR audio.

The VocalFusion XVF3510-UA voice processor implements a full-speed USB 2.0 compliant device supporting USB Audio Class 1.0 at 16kHz and 48kHz sample rates with resolutions of 16, 24 or 32 bits. An internal audio crossbar switch allows the selectable output of processed channels, raw microphones, reference audio loopback audio. The USB device also provides HID and Endpoint 0 control interfaces as detailed below.

The VocalFusion XVF3510-UA voice processor provides the following additional interfaces to increase usability and reduce total system cost:

- Four General Purpose Output pins. These can be configured as simple digital I/O pins, Pulse Width Modulated (PWM) outputs and rate adjustable LED flashers.
- Four General Purpose Input pins. These can be used as simple logic inputs or event capture (edge detection). Separate USB HID events can be triggered based on two input pins to provide interrupt detection from connected peripherals and pushbuttons.
- SPI master interface to control and interrogate an SPI slave device, such as ADCs, DACs or external keyword detection devices.
- I2C master interface to control and interrogate multiple I2C based devices allowing control of peripherals such as ADCs and DACs.
- I2S master for optional input of the AEC reference, and output of audio data from the on-chip audio crossbar.

The VocalFusion XVF3510-UA voice processor can be booted over SPI by a local host processor or from a separate, user supplied, QSPI Flash memory. When operating with flash, the memory can be used for the following functions:

- A default firmware image for power on operation.
- An upgrade image. Upgrades are provided via a USB control path on USB Endpoint 0 providing a host-controlled upgrade processes for Over-The-Air Device Management.
- Persistent user information space to allow user configured data such as board identifiers and serial numbers maintained across multiple firmware upgrade cycles.
- An upgradable user command space. Commands stored in this space are executed at boot time, allowing the definition of the startup behaviour, tuning and configuration of the VocalFusion XVF3510 as well as the configuration of I2C/SPI peripheral devices connected to it.

With the exception of the persistent user information, the contents of the flash and therefore the configuration of the system can be upgraded and configured using the Device Firmware Upgrade (DFU) mechanism from the host processor.

The VocalFusion XVF3510-UA voice processor is supplied in a 7mm x 7mm 60pin QFN package and has a typical power consumption 500mW during active processing.

1.2. XVF3510 AUDIO PROCESSING PIPELINE

The XVF3510 audio processing pipeline takes inputs from a pair of MEMS Pulse Density Modulation (PDM) microphones and uses advanced signal processing to create audio streams suitable for use in Automatic Speech Recognition (ASR) and voice communication applications. The block diagram of this audio processing pipeline is shown in the figure below.

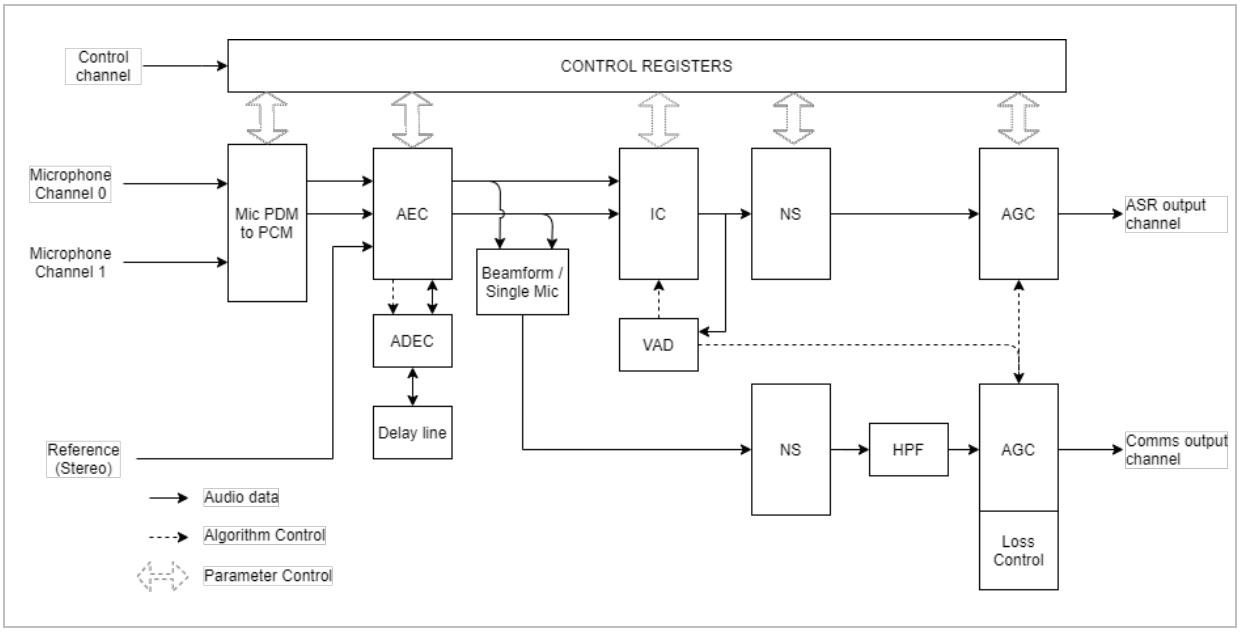


Figure 1-2 XVF3510 audio processing pipeline

The pipeline enhances the captured audio stream using a set of complementary signal enhancement and noise reduction processes:

- **Microphone Pulse Density Modulation (PDM) to Pulse Code Modulation (PCM) conversion:** Converts the PDM audio input from the microphones into PCM format allowing further processing.
- **Acoustic Echo Cancellation (AEC):** enables the XVF3510 to detect voice signals in the presence of high volume, stereo audio from the product in to which it is integrated. This process takes the stereo audio from the product as a reference signal and models the echo characteristics between each speaker and microphone caused by the acoustic environment of the device and room. These four models are used to continuously remove the echoes from out the audio outputs from the microphone audio input. The models are continuously adapted to the acoustic environment to accommodate changes in the room created by events such as doors opening or closing and people moving in the room.
- **The Automatic Delay Estimation Control (ADEC):** automatically monitors and manages the delay between the reference audio and the echo received by the microphone to ensure optimal AEC cancellation when the audio output latency is variable or non-zero.
- **Interference Cancellation (IC):** suppresses static noise from point sources such as cooker hoods, washing machines, or radios for which there is no reference audio signal available. When an internal Voice Activity Detector (VAD) indicates the absence of voice, the IC adapts to suppress point noise sources in the environment. When voice is detected adaption is suspended maintaining suppression of the interfering noise source.

- **Noise Suppression (NS):** suppresses diffuse noise from sources whose frequency characteristics do not change rapidly over time such as air conditioning or city background noise.
- **Automatic Gain Control (AGC):** tunes separate AGC channels for Automatic Speech Recognition (ASR) and communications output. The internal VAD is used to prevent gain changes in the ASR output channel during speech to improve speech recognition performance.

1.3. REFERENCE SIGNAL DELAY

As shown above, the XVF3510 includes an Automatic Delay Estimator Control (ADEC) which is used to time-align the reference and microphone signals, allowing the AEC to work effectively. This is an essential aspect of device operation for situations where the audio output path is unknown, such as in TVs and set-top box architectures.

The ADEC applies a time shift to one of the signals based on an automatic estimate between them or a user-defined delay, to deliver a synchronised input to the AEC.

A delay of between 0-150ms can be applied to either the reference signal or microphone input, equivalent to 0-2400 samples at 16kHz sample frequency.

The ADEC runs in one of three modes:

- Automatic - the ADEC runs immediately the device starts. It constantly monitors the reference signal and microphone input for changes of time alignment and automatically adjusts its delay as necessary.
- Manual – in this mode, the ADEC waits in a disabled state until the device is manually triggered by the host. The delay is estimated at the trigger point, or a selected fixed delay applied. The delay set will be used until it is changed by:
  - manually applying a different fixed delay;
  - manually triggering a new delay estimate;
  - switching to automatic mode.
- Estimate on Start-up (default) - The ADEC runs immediately the device starts, calculates the delay between the two signals and applies that delay to all subsequent signals. After making the initial delay estimate and delay setting, no further changes will be made unless manually triggered or automatic mode is selected.

For further information on the usage of ADEC please refer to the XVF3510 User Guide.

1.4. EXAMPLE APPLICATION

The figure below shows the essential components and signals for a XVF3510-UA application using QSPI flash memory.

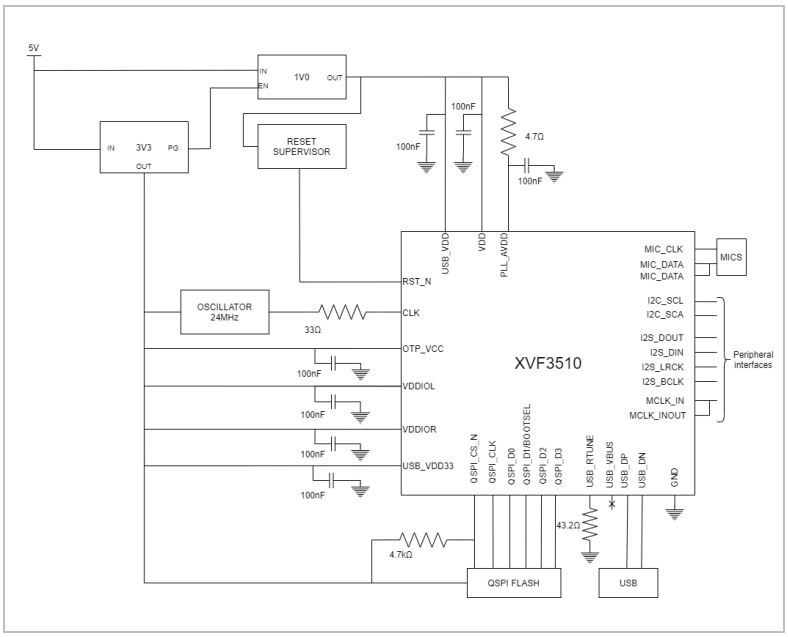


Figure 1-3 Essential components of a XVF3510-UA application booted from a QSPI flash

2. PIN DIAGRAM

2.1. PIN CONFIGURATION

The pinout of the XVF3510-UA including all optional interfaces is shown in the figure below.

Pins marked RESVD are internally connected and should remain unconnected

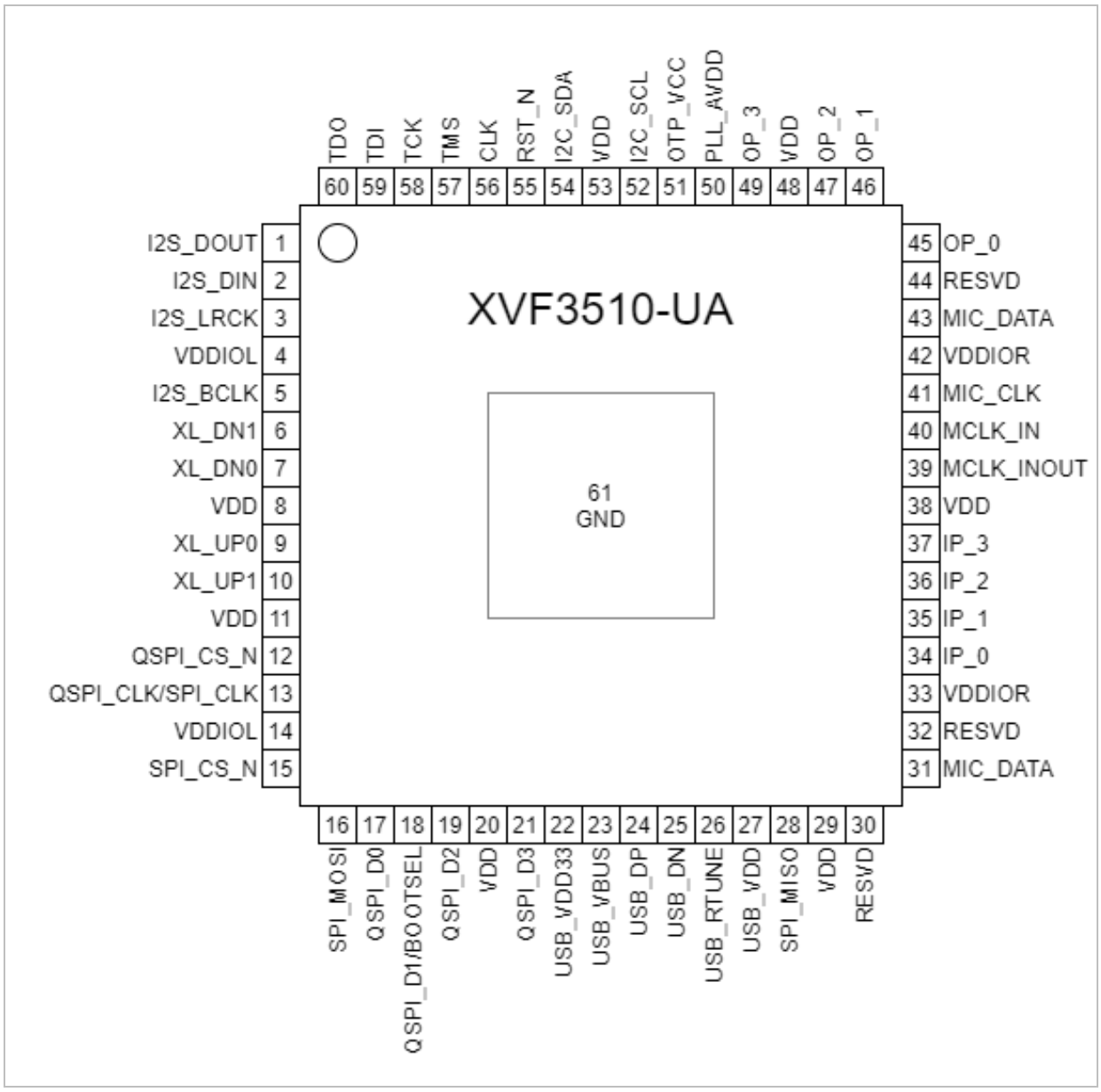


Figure 2-1 VocalFusion XVF3510-UA pin configuration

2.2. SIGNAL DESCRIPTION

The table below lists the functions of all the pins shown in the figure above.

Table 2-1 XVF3510-UA pin functions

NAME	PIN	TYPE	DESCRIPTION	NOTE
I2S_DOUT	1	O	Peripheral I2S Master - I2S data out	
I2S_DIN	2	I	Peripheral I2S Master - I2S data input. Configurable as AEC reference source. See user guide for further information.	
I2S_LRCK	3	O	Peripheral I2S Master - I2S left-right clock.	
VDDIOL	4, 14	PWR	Digital I/O power left. 3.3V (nominal)	A
I2S_BCLK	5	O	Peripheral I2S Master - I2S bit clock.	
XL_DN1	6	I/O	XMOS link, downlink bit 1	
XL_DN0	7	I/O	XMOS link, downlink bit 0	
VDD	8, 11, 20, 29, 38, 48, 53	PWR	Digital core power. 1.0V (nominal)	A
XL_UP0	9	I/O	XMOS link, uplink bit 0.	
XL_UP1	10	I/O	XMOS link, uplink bit 1.	
QSPI_CS_N	12	I/O	QSPI Boot Flash - Chip Select. This pin should be pulled high externally to the device using a 4.7k ohm resistor.	
QSPI_CLK/SPI_CLK	13	I/O	QSPI Boot Flash - QSPI Clock and SPI Clock	
SPI_CS_N	15	I/O	Slave SPI boot / Peripheral SPI Master - Chip Select This pin should be pulled high externally to the device using a 4.7k ohm resistor. NOTE: When slave boot is enabled the SPI interface operates as a slave prior to and during boot image transfer. Once complete, the SPI interface becomes a Master and can be used to interface to peripheral devices.	
SPI_MOSI	16	I/O	Peripheral SPI Master - SPI Master Out Slave In NOTE: When slave boot is enabled the SPI interface operates as a slave prior to and during boot image transfer. Once complete, the SPI interface becomes a Master and can be used to interface to peripheral devices.	
QSPI_D0	17	I/O	QSPI Boot Flash - QSPI Data Line 0	
QSPI_D1/BOOTSEL	18	I/O	QSPI Boot Flash - QSPI Data Line 1 and Boot selection. If this pin is tied high via a 4.7k ohm resistor on startup, the device will enable SPI slave boot mode. If the pin is left floating, pulled low or connected to a quad SPI D1 pin, the device will start in QSPI master mode and boot from QSPI flash memory.	
QSPI_D2	19	I/O	QSPI Boot Flash - QSPI Data Line 2	
QSPI_D3	21	I/O	QSPI Boot Flash - QSPI Data Line 3	

NAME	PIN	TYPE	DESCRIPTION	NOTE
USB_VDD33	22	PWR	Analogue supply to the USB-PHY. 3.3V (nominal)	A
USB_VBUS	23	I	USB VBUS Voltage. NOTE: Self-powered operation is not supported by device firmware, and therefore this pin should not be connected. For further details refer to the USB Device section in Device Interfaces.	
USB_DP	24	I/O	USB positive data line	
USB_DN	25	I/O	USB negative data line	
USB_RTUNE	26	I	USB tuning resistor. Connect a 43.2 ohm resistor to ground	
USB_VDD	27	PWR	Digital supply to the USB-PHY. 1.0V (nominal)	A
SPI_MISO	28	I/O	Peripheral SPI Master - SPI Master In Slave Out NOTE: When slave boot is enabled the SPI interface operates as a slave prior to and during boot image transfer. Once complete, the SPI interface becomes a Master and can be used to interface to peripheral devices.	
MIC_DATA	31, 43	I	Mic array data NOTE: Pin 43 and Pin 31 should be connected together by a trace on the PCB.	B
VDDIOR	33, 42	PWR	Digital I/O power right. 3.3V (nominal)	A
IP_0	34	I	General purpose input 0	
IP_1	35	I	General purpose input 1	
IP_2	36	I	General purpose input 2	
IP_3	37	I	General purpose input 3	
MCLK_INOUT	39	O	MCLK_INOUT outputs the Master audio clock (MCLK), nominally 24.576MHz. The clock adapts it frequency to match the host audio clock by inferring the sample frequency from USB data rate. NOTE: MCLK_IN and MCLK_INOUT should be connected via short track externally to the device.	
MCLK_IN	40	I	MCLK_IN is used to derive the microphone sample clock and must be driven by the MCLK_INOUT output. NOTE: MCLK_IN and MCLK_INOUT should be connected via short track externally to the device.	
MIC_CLK	41	O	Mic array clock. This 3.072MHz clock output drives the data capture from the PDM microphones.	B
OP_0	45	O	General purpose output 0	
OP_1	46	O	General purpose output 1	
OP_2	47	O	General purpose output 2	
OP_3	49	O	General purpose output 3	

NAME	PIN	TYPE	DESCRIPTION	NOTE
PLL_AVDD	50	PWR	PLL analogue power. This 1.0V (nominal) supply should be separated from the other supplies at the same voltage by a low pass filter.	A
OTP_VCC	51	PWR	OTP power. 3.3V (nominal)	A
I2C_SCL	52	O	Peripheral I2C Master - I2C serial clock line	
I2C_SDA	54	I/O	Peripheral component I2C serial data line	
RST_N	55	I	Device reset - active low. This pin has a Schmitt trigger input and an internal weak pull-up resistor.	
CLK	56	I	Processor reference clock. This input pin has a Schmitt trigger input. A 24MHz reference clock must be provided to this pin.	
TMS	57	I	JTAG Test mode select. This pin has a weak pull-up resistor applied during and after reset until the device has booted.	
TCK	58	I	JTAG Test clock. This pin has a Schmitt trigger input and a weak pull-down resistor applied during and after reset until the device has booted.	
TDI	59	I	JTAG Test data input. This pin has a weak pull-up resistor applied during and after reset until the device has booted.	
TDO	60	O	JTAG Test data output. This pin has a weak pull-down resistor applied during and after reset until the device has booted.	
GND	61 (Paddle)	GND	Ground	A
RESERVED	30, 32, 44	RSVD	Do not connect to these pins	

A: All power pins must be connected

B: Two standard PDM MEMS microphones should be connected to the MIC_DATA pins. The MIC_DATA line is shared, and the microphone data read on alternative edges of the MIC_CLK signal. One microphone should be set to be left (output on rising edge of clock) and the other right (rising on the falling edge of clock).

3. DEVICE INTERFACES

3.1. INTEGRATED USB INTERFACE

USB Audio Class 1.0 running at Full Speed (12Mbps) is used to deliver processed voice audio to the host processor, stereo reference audio from the host and as a control interface. In this mode the adaptive USB Audio endpoint is used to generate an MCLK synchronised to the USB host. This is driven out of MCLK_INOUT which must be connected to MCLK_IN via a PCB trace outside the device. The table below shows the signals required to implement a USB interface using the XVF3510:

Table 3-1 USB connections

NAME	DESCRIPTION	PIN
USB_DP	Connect to USB connector	24
USB_DN	Connect to USB connector	25
USB_RTUNE	An external resistor of 43.2 ohm (1% tolerance) should connect USB_RTUNE to ground, as close as possible to the device.	26
USB_VBUS	USB VBUS. Self-powered operation is not supported by device firmware, and therefore this pin should not be connected.	23
USB_VDD	1.0V digital supply. This 1V0 (nominal) supply may be powered directly by the same regulator used to power VDD. USB_VDD is required even if the USB interface is not used.	27
USB_VDD33	3.3V analogue supply to the USB-PHY. USB_VDD33 is required even if the USB interface is not used.	22

The XVF3510-UA supports USB bus-powered operation.

XMOS recommends that the USB_VBUS is not connected when the device is wholly powered by USB. A typical schematic is shown below.

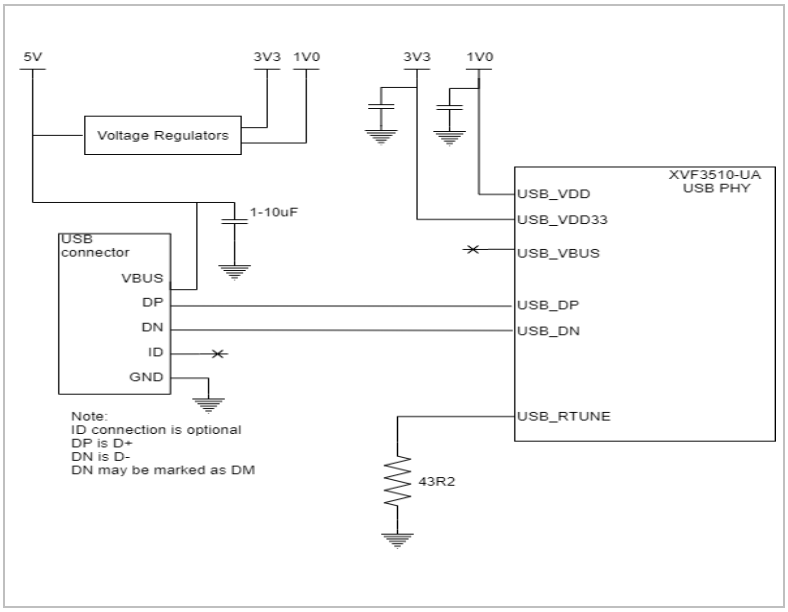


Figure 3-1 Bus-powered USB design

3.2. PDM MICROPHONE INPUTS

Two standard PDM MEMS microphones should be connected to the MIC_DATA pins. Both MIC_DATA pins must be connected together. The data input makes use of the left and right channel output capability of standard MEMS microphones and the microphone data is read on alternative edges of the MIC_CLK signal. The XVF3510 reads one microphone on the positive edge of the microphone clock and the other microphone on the negative edge of the clock.

The XVF3510 outputs a microphone clock at 3.072MHz, which is fed directly to both microphones. This clock is divided down from the MCLK_IN pin (pin 40) which must be connected to MCLK_INOUT (pin 39). This signal must be used to clock the microphone PDM output to avoid undefined artifacts in the processed audio stream. One microphone should be set to be left (output on rising edge of clock) and the other right (output on the falling edge of clock).

An example microphone circuit is shown in the figure below:

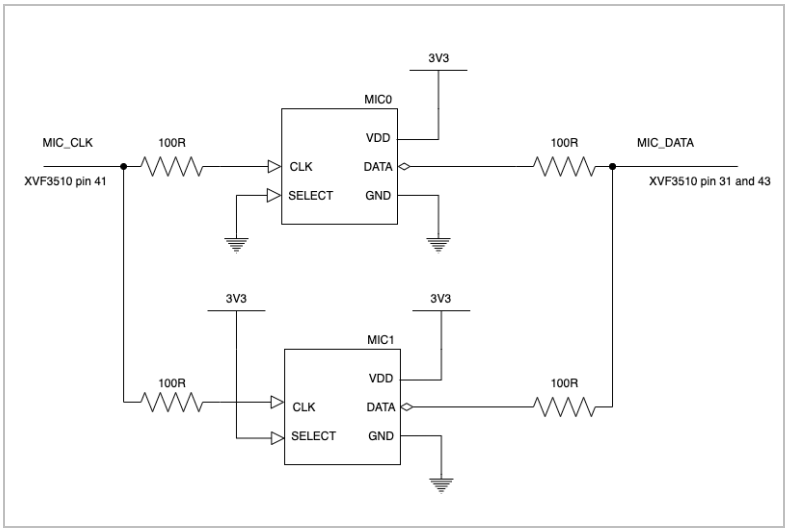


Figure 3-2 PDM microphone schematic

The voice processor has been tested and characterised with microphones placed with a 71mm separation and connected to the product casing in such a way that the audio path to each microphone from outside the product is independent. The XVF3510 algorithms automatically adapt to alternative spacing, but differences in audio performance may occur and should be thoroughly characterised.

3.3. QSPI

When QSPI boot mode is enabled (default), the XVF3510 enables the six QSPI pins, see table below, and drives the QSPI clock as a QSPI Master. A READ command is issued with a 24-bit address 0x000000.

Table 3-2 QSPI signals

SIGNAL	DESCRIPTION	COMMENT	PIN
QSPI_CS_N	QSPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	12
QSPI_CLK/SPI_CLK	QSPI Clock		13
QSPI_D0	QSPI Data Line 0		17
QSPI_D1/BOOTSEL	QSPI Data Line 1 and boot selection.	If pin is tied high via a 4.7k ohm resistor on startup, the device will start in SPI slave boot mode. If the pin is left floating, pulled low or connected to a quad SPI D1 pin on a memory device, the device will start in QSPI master mode and attempt to boot from a local QSPI flash memory.	18
QSPI_D2	QSPI Data Line 2		19
QSPI_D3	QSPI Data Line 3		21

The XVF3510 expects each byte to be transferred with the least-significant nibble first. Programmers that write bytes into a QSPI interface using the most significant nibble first may have to reverse the nibbles in each byte of the image stored in the QSPI device. When bulk programming flash devices the Quad Enable bit in the flash setting register should be set.

3.4. SPI

The SPI interface can be utilised in both Master and Slave configurations for peripheral control of components like DACs and ADCs (Master), and SPI boot from host a host processor (Slave).

3.4.1. PERIPHERAL COMPONENT CONTROL

Once the XVF3510 has successfully booted, the SPI interface can be used to configure peripheral components such as DACs, ADCs and keyword detection devices. In this mode the SPI interface operates as a master, and transfers data held in flash, or received from the host over the control interface. The interface operates with the following specifications:

- 1MHz SPI clock
- Up to 128 bytes SPI write
- Up to 56 bytes SPI read

For further information on this configuration consult the XVF3510 user guide.

3.4.2. SPI SLAVE BOOT

To enable the SPI boot from an external host processor, the QSPI_D1/BOOTSEL should be pulled to VDDIO on power-up. This activates the SPI interface, which operates as a slave to the host processor for the transfer of the boot image, which is clocked in with the least significant bit first in each transferred byte.

This is an alternative to using an attached QSPI flash to automatically transfer boot data on startup.

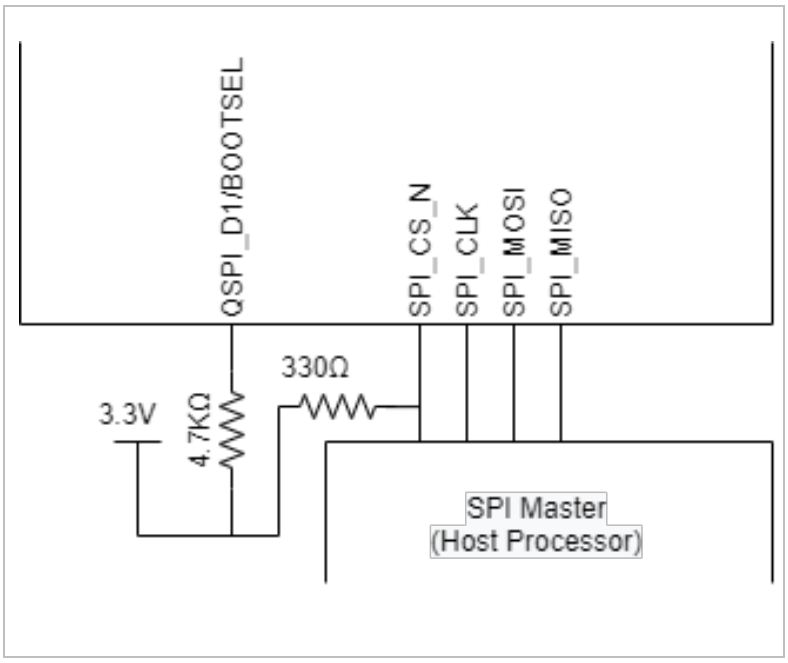


Figure 3-3 XVF3510 SPI slave boot configuration

NOTE: Care should be taken when both SPI slave boot and SPI peripheral control are present in the same system to avoid unintended interaction between the host, XVF3510 and other peripheral components.

The SPI pins are shown below in the table below.

Table 3-3 SPI signals

SIGNAL	DESCRIPTION	COMMENT	PIN
SPI_CLK	SPI Clock		13
SPI_CS_N	SPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor	15
SPI_MOSI	SPI Master Out Slave In		16
SPI_MISO	SPI Master In Slave Out		28

3.4.3. I2S INTERFACE

The XVF3510-UA operates as an I2S Master to output audio to peripheral devices or optionally receive reference audio signal instead of over USB. This bidirectional flow of audio samples must be synchronised to a single set of I2S clocks as shown in the table below.

Table 3-4 I2S signals

SIGNAL	DESCRIPTION	COMMENT	PIN
MCLK_INOUT	Master clock output	Configurable to 6.144MHz, 12.288MHz or 24.576MHz	39
I2S_BCLK	I2S bit synchronisation clock	3.072MHz or 1.024MHz clock derived from MCLK_INOUT	5
I2S_LRCK	I2S sample synchronisation clock	48kHz or 16kHz clock derived as BLCK/64	3
I2S_DIN	I2S Data in	Reference audio data from I2S device	2
I2S_DOUT	I2S Data Out	Audio data out to a peripheral device	1

The I2S audio samples are transmitted serially with a one I2S_BCLK delay between the change of I2S_LRCK phase and the start (MSB) of the audio sample for that channel. This the standard alignment for I2S systems.

3.5. I2C INTERFACE

The peripheral I2C interface can be utilised to connect to peripheral components such as DACs, ADCs or companion devices for setup and control. The control messages can be defined to be read from flash, or by direct host control. The interface operates with the following specifications:

- 100 kbps SCL clock speed
- Register read/write
- Up to 56 byte I2C read/write

See the XVF3510 user guide for further information.

Table 3-5 Peripheral I2C Master connections

SIGNAL	DESCRIPTION	COMMENT	PIN
I2C_SCL	I2C serial clock line	Must be externally pulled up to VDDIO	52
I2C_SDA	I2C serial data line	Must be externally pulled up to VDDIO	54

3.6. GENERAL-PURPOSE INPUT/OUTPUT

Four input and four output pins are provided to allow general-purpose I/O such as LEDs and button controls. Input pins can be individually read by the host using the control interface and configured to detect edge events. The output pins can be individually set and they have configurable Pulse Width Modulated (PWM) brightness control with blinking sequences.

The GPIO pins are shown in the table below.

Table 3-6 GPIO pin table

NAME	DESCRIPTION	PIN	I/O
IP_0	General purpose input	34	I
IP_1	General purpose input	35	I
IP_2	General purpose input	36	I
IP_3	General purpose input	37	I
OP_0	General purpose output	45	O
OP_1	General purpose output	46	O
OP_2	General purpose output	47	O
OP_3	General purpose output	49	O

For more information please refer to the XVF3510 User Guide.

4. DEVICE OPERATION

4.1. POWER SUPPLIES

The XVF3510 has the following power supply pins:

Table 4-1 Power Pins

NAME	DESCRIPTION	PIN
VDD	Digital core power. 1.0V (nominal)	8, 11, 20, 29, 38, 48, 53
VDDIOL	Digital I/O power left. 3.3V (nominal)	4, 14
VDDIOR	Digital I/O power right. 3.3V (nominal)	33, 42
PLL_AVDD	PLL analogue power. This 1.0V (nominal) supply should be separated from the other supplies at the same voltage by a low pass filter.	50
OTP_VCC	One Time Programmable Memory power. 3.3V (nominal)	51
USB_VDD	Digital supply to the USB-PHY. 1.0V (nominal)	27
USB_VDD33	Analogue supply to the USB-PHY. 3.3V (nominal)	22
GND	Ground	61 (Paddle)

NOTE: All power pins must be connected

Several pins of each type are provided to minimise the effect of inductance within the package, all of which must be connected. The power supplies must be brought up monotonically within 10ms and input voltages must not exceed specification at any time.

VDDIO/OTP_VCC and VDD can ramp up independently. In order to reduce stresses on the device, it is preferable for them to ramp up in a short time frame of each other, no more than 50 ms apart. RST_N should be kept low until all power supplies are stable and within tolerances of their final voltage.

When RST_N comes up, the processor will attempt to boot within a very short period of time. If booting from external flash, ensure that there is enough time between before RST_N coming up for the external flash to settle as shown below.

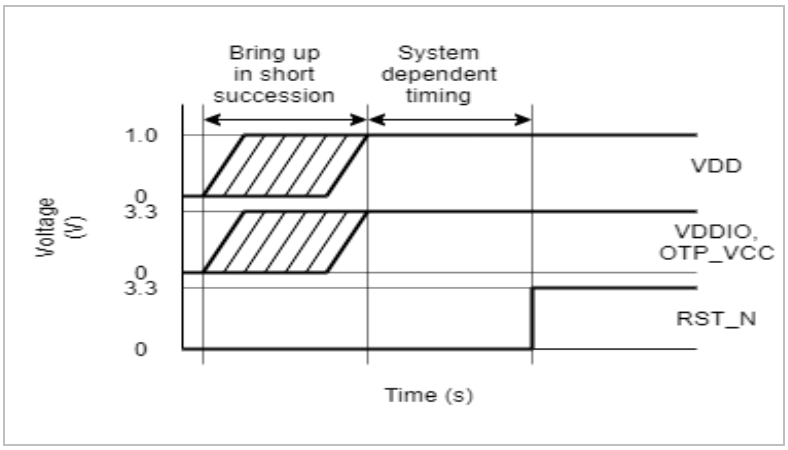


Figure 4-1 Sequencing of power supplies and RST_N

The PLL_AVDD supply should be separated from the other noisier supplies on the board. The PLL requires a very clean power supply, and a low pass filter (for example, a 4.7 ohm resistor and 100nF multi-layer ceramic capacitor) is recommended on this pin.

A single ground pin is provided as the central paddle pin beneath the device in the package. It is recommended that this is connected by a minimum of 10 evenly spaced vias to the board ground plane.

The VDD and VDDIO supplies should be decoupled close to the chip by several 100nF low inductance multi-layer ceramic capacitors between the supplies and GND (for example, 100nF 0402 for each supply pin). The ground side of the decoupling capacitors should have as short a path back to the GND pins as possible. A bulk decoupling capacitor of at least 10uF should be placed on each of these supplies.

4.2. CLOCKS

The XVF3510 must be provided with a 24MHz clock signal as shown below.

Table 4-2 XVF3510 clock signals

SIGNAL	DESCRIPTION	COMMENT	PIN
CLK	Master clock (system)	24MHz clock signal	56

4.3. RESET

The XVF3510 uses an active low RST_N pin to reset the device. On power-up hold RST_N low until the power supplies have stabilised to within operating conditions. Once RST_N is de-asserted the device boot process will commence within T(INT). See switching characteristics for further information.

Table 4-3 Reset Signal

SIGNAL	DESCRIPTION	COMMENT	PIN
RST_N	Device reset	Active low	55

4.4. BOOT MODES

On startup and after a reset event, the XVF3510 is booted either using an externally connected QSPI flash memory or by transferring a boot image to the device via SPI from a host processor.

SLAVE BOOT MODE

The boot mode is specified using QSPI_D1/BOOTSEL. If this pin is tied high via a 4.7k ohm resistor on startup, the XVF3510 will enable SPI Slave boot mode and activate the pins shown below.

Table 4-4 SPI Slave boot pins

SIGNAL	DESCRIPTION	COMMENT	PIN
QSPI_CLK/SPI_CLK	SPI Clock		13
SPI_CS_N	SPI Chip Select	Pull high externally to the device using a 4.7k ohm resistor.	15
SPI_MOSI	SPI Master Out Slave In		16
SPI_MISO	SPI Master In Slave Out		28

QSPI MASTER BOOT MODE

If the QSPI_D1/BOOTSEL pin is connected to a QSPI_D1 pin on a flash device, the XVF3510 will boot from a local QSPI flash in QSPI Master mode. The active pins are shown below.

Table 4-5 QSPI Master peripheral interface pins

NAME	DESCRIPTION	PIN	I/O
QSPI_CS_N	QSPI Chip Select. This pin should be pulled high externally to the device using a 4.7k ohm resistor.	12	I/O
QSPI_D0	QSPI Data Line 0	17	I/O
QSPI_D1 / BOOTSEL	QSPI Data Line 1 and boot selection. To activate QSPI master boot mode connect directly to QSPI Data Line 1 on Quad capable flash device.	18	I/O
QSPI_D2	QSPI Data Line 2	19	I/O
QSPI_D3	QSPI Data Line 3	21	I/O
QSPI_CLK / SPI_CLK	QSPI Clock and SPI Clock	13	I/O

4.5. QSPI FLASH SUPPORT

The device firmware has been tested using Adesto SPI Serial Flash Memory (AT25SF161). Other flash devices, which conform to the following specification may also be used:

Table 4-6 Flash device specification supported by XVF3510

DEVICE CHARACTERISTIC	DESCRIPTION	VALUE
Page size	Size of flash page in bytes	256
Number of pages	Total number of pages	8192
Address size	Number of bytes used to represent the address	3
Read ID operation code	Operation code to read the device identification (ID) information	0x9F
Read ID dummy bytes	Number of dummy bytes after read command before ID is returned	0
ID size	Size of ID in bytes	3
Sector Erase operation code	Operation code for 4 KB Erase	0x20
Sector information	Arrangement of sectors	Regular (all equally sized - 4KB)
Write Enable operation code	Operation code for write enable	0x06
Write Disable operation code	Operation code for write disable	0x04
Page Program operation code	Operation code for page program	0x02
Fast Quad Read operation code	Operation code for Fast Quad I/O Read	0xEB
Fast Quad Read dummy bytes	Number of dummy bytes after setup of fast quad read that data is returned	1
Read Status Register operation code	Operation code for reading status register	0x05
Write Status Register operation code	Operation code for write to the status register	0x01
Write Status Register Busy Mask	Bit mask for operation in progress (device busy)	0x01

4.6. DEVICE FIRMWARE

Device Firmware Upgrade (DFU) is supported for devices that have QSPI flash connected and loaded with a firmware image. If the DFU process fails, the boot process safely falls back to the factory image allowing the user to re-attempt the upgrade. Images loaded via DFU can also be removed allowing the device to revert to the factory image.

For further information on the operation of the DFU mechanism refer to the XVF3510 User Guide.

5. ELECTRICAL CHARACTERISTICS

5.1. ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. Exposure to any absolute maximum rating condition for extended periods may affect device reliability and lifetime.

Table 5-1 Absolute maximum ratings

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
VDD	Core supply voltage	-0.2	1.1	V	
PLL_VDD	PLL analogue supply	-0.2	1.1	V	
VDDIOL, VDDIOR	I/O supply voltage	-0.3	3.75	V	
OTP_VCC	OTP supply voltage	-0.3	3.75	V	
Tj	Junction temperature	-	125	°C	
Tstg	Storage temperature	-65	150	°C	
V(Vin)	Voltage applied to any I/O pin	-0.3	3.75	V	
I(GPOn)	General purpose output pin current	-30	30	mA	
I(VDDIOL)	Current for VDDIOL per signal pin	-	490	mA	A, B, C
I(VDDIOR)	Current for VDDIOR per signal pin	-	490	mA	A, B, C
USB_VDD	USB DC supply voltage	-0.2	1.1	V	
USB_VDD33	USB analog supply voltage	-0.3	3.75	V	
USB_VBUS	USB VBUS voltage	-0.3	5.75	V	
USB_DP	USB DP voltage	-0.3	5.5	V	
USB_DM	USB DM voltage	-0.3	5.5	V	

A: Exceeding these current limits will result in premature ageing and reduced lifetime.

B: This current consumption must be evenly distributed over all VDDIO pins

C: All main power (VDD, VDDIO) and ground (VSS) pins must always be connected to the external power supply, in the permitted range.

5.2. OPERATING CONDITIONS

Table 5-2 Operating conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VDD	Tile DC supply voltage	0.95	1.00	1.05	V	
VDDIOL	I/O supply voltage	3.135	3.30	3.465	V	

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
VDDIOR	I/O supply voltage	3.135	3.30	3.465	V	
USB_VDD	USB tile DC supply voltage	0.95	1.00	1.05	V	
USB_VDD33	USB peripheral supply	3.135	3.30	3.465	V	
PLL_AVD	PLL analogue supply	0.95	1.00	1.05	V	
Ta	Ambient operating temperature (Commercial)	0	-	70	°C	
Tj	Junction temperature	-	-	125	°C	

5.3. POWER CONSUMPTION

Table 5-3 Power consumption

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
I(DDCQ)	Quiescent VDD current	-	20	-	mA	A, B, C, F
PD	Active power dissipation - USB	-	500	-	mW	A
IDD	Active VDD current	-	420	550	mA	A, D
I(ADDPLL)	PLL_AVDD current	-	5	7	mA	E
I(VDD33)	VDD33 current	-	53.4	-	mA	
I(USB_VDD)	USB_VDD current	-	16.6	-	mA	

A: Use for budgetary purposes only.

B: Assumes no active clock inputs.

C: Includes PLL current.

D: Measurement conditions: VDD = 1.0 V, VDDIO = 3.3 V, 25 °C, 500 MHz, average device resource usage.

E: PLL_AVDD = 1.0 V

F: Provided for an indication of power when the device is held in reset

5.4. DC CHARACTERISTICS

Table 5-4 DC characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V(IH)	Input high voltage	2.00		3.60	V	A
V(IL)	Input low voltage	-0.30		0.70	V	A
V(OH)	Output high voltage	2.20			V	B
V(OL)	Output low voltage			0.40	V	B
I(PU)	Internal pull-up current (Vin=0V)	-100			µA	C
I(PD)	Internal pull-down current (Vin=3.3V)			100	µA	C
I(LC)	Input leakage current	-10		10	µA	

A: All pins except power supply pins.

B: Measured with 4 mA drivers sourcing 4 mA

C: Used to guarantee logic state for an I/O when high impedance. The internal pull-ups/pull-downs should not be used to pull external circuitry. In order to pull the pin to the opposite state, a 4.7KΩ resistor is recommended to overcome the internal pull current.

5.5. ESD STRESS VOLTAGE

Table 5-5 ESD stress voltage

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
HBM	Human body model	-2.00		2.00	kV	
CDM	Charged device model	-500		500	V	

6. SWITCHING CHARACTERISTICS

6.1. RESET

Table 6-1 Reset timing requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
Reset pulse width	T(RST)	5	-	-	us	
Initialisation time	T(INT)	-	-	150	us	A

A: Time taken to start boot up procedure after RST_N is de-asserted

6.2. CLOCK

Table 6-2 Master clock switching requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
Clock input frequency	f	24	-	24	MHz	A
Slew rate	SR	0.10	-	-	V/ns	
Long term jitter (pk-pk)	TJ(LT)	-	-	2	%	B

A: Less than ±100ppm frequency tolerance

B: Percentage of CLK period

6.3. JTAG TIMING

Table 6-3 JTAG timing requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
TCK frequency (debug)	f(TCK_D)	-	-	18	MHz	
TCK frequency (boundary scan)	f(TCK_B)	-	-	10	MHz	
TDO to TCK setup time	T(SETUP)	5	-	-	ns	A
TDO to TCLK hold time	T(HOLD)	5	-	-	ns	A
TCK to output delay	T(DELAY)	-	-	15	ns	B

A: Timing applies to TMS and TDI inputs

B: Timing applies to TDO output from negative edge of TCK

6.4. QSPI MASTER (EXTERNAL FLASH FOR BOOT IMAGE STORAGE)

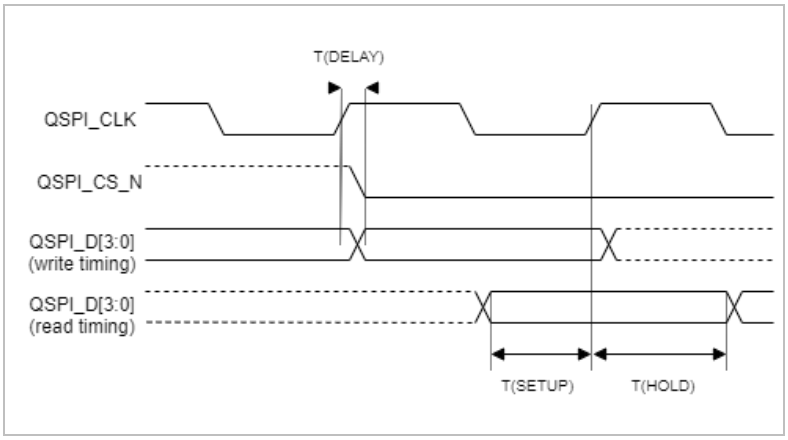


Figure 6-1 QSPI timing

Table 6-4 QSPI timing requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS
QSPI Clock frequency	f(QSPI_CLK)	-	TBC	50	MHz
QSPI_CLK to QSPI Data output delay	T(DELAY)	-2.7	-	2.7	ns
QSPI Data input to QSPI_CLK setup time	T(SETUP)	21.3	-	-	ns
QSPI Data input to QSPI_CLK hold time	T(HOLD)	-11	-	-	ns

6.5. USB

Bus timings and signalling properties are fully compliant with the USB 2.0 specification. For further information refer to the specification available from https://www.usb.org

6.6. I2S MASTER

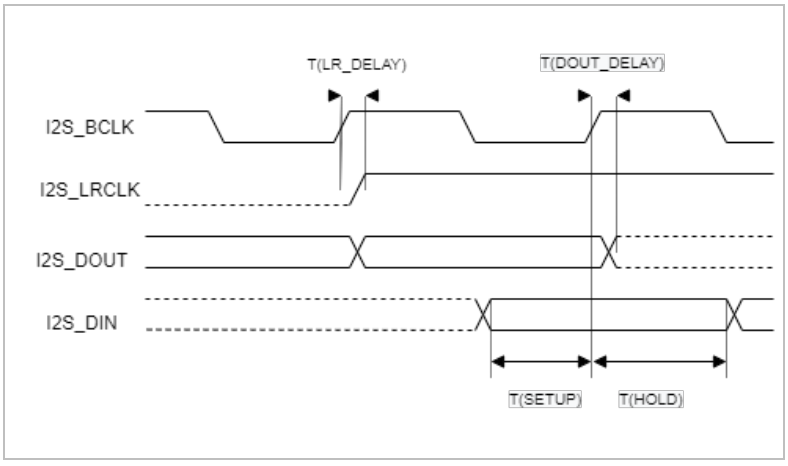


Figure 6-2 I2S master timing

Table 6-5 I2S master timing requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
Master clock output frequency1	f(MCLKout)	6.144	-	24.576	MHz	A
Master clock output jitter (pk-pk)	T(Jitter)	TBC	-	TBC	ns	
Master clock output instantaneous drift	f(IDrift)	TBC	-	TBC	MHz	
Master clock output long term drift	f(LTDrift)	-	-	0	MHz	
I2S Bit Clock frequency output	f(I2S_BCLK)	1.024	-	3.072	MHz	B
I2S_BCLK to I2S sample clock (LR_CLK) output delay	T(LR_DELAY)	-2.7	-	2.7	ns	
I2S_BCLK to I2S data output delay	T(DOUT_DELAY)	-2.7	-	2.7	ns	
I2S_Data input to I2S_BCLK setup time	T(SETUP)	21.3	-	-	ns	
I2S_Data input to I2S_BCLK hold time	T(HOLD)	-11	-	-	ns	

A: Configurable output divider based on derived audio sample rate (16kHz / 48kHz)

B: Operation configurable for 16kHz and 48kHz

6.7. SPI SLAVE (EXTERNAL PROCESSOR BOOT)

Table 6-6 SPI slave timing requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
SPI Clock frequency	f(SPI_CLK)	-	TBC	TBC	MHz	
SPI_CLK to MISO output delay	T(DELAY)	11	-	21.3	ns	
SPI Master Output Slave Input (MOSI) to SPI_CLK setup time	T(SETUP)	0	-	-	ns	
SPI Master Output Slave Input to (MOSI) SPI_CLK hold time	T(HOLD)	6	-	-	ns	

A: Timing also applies to SPI Chip Select input (SPI_CS_N)

6.8. SPI MASTER (PERIPHERAL CONTROL)

Table 6-7 SPI master timing requirements

PARAMETER	SYMBOL	MIN	TYPICAL	MAX	UNITS	NOTES
SPI Clock frequency	f(SCLK)	-	TBC	TBC	MHz	
SPI CLK to SPI Master In Slave Out (MOSI) output delay	T(DELAY)	-2.7	-	2.7	ns	A
SPI Master Out Slave In (MISO) setup time	T(SETUP)	21.3	-	-	ns	
SPI Master Out Slave In (MISO) hold time	T(HOLD)	-11	-	-	ns	

A: Timing also applies to SPI Chip Select input (SPI_CS_N)

7. DESIGN GUIDELINES

7.1. INTEGRATED USB PHY

The USB_DP and USB_DN lines are the positive and negative data polarities (D+/D-) of a full speed USB signal respectively. Their high-speed differential nature implies that they must be coupled and properly isolated. The board design must ensure that the board traces for USB_DP and USB_DN are tightly matched. In addition, according to the USB 2.0 specification, the USB_DP and USB_DN differential impedance must be 90 Ω.

The following guidelines will help to avoid signal quality and EMI problems on high-speed USB designs. They relate to a four-layer (Signal, Ground, Power, Signal) PCB.

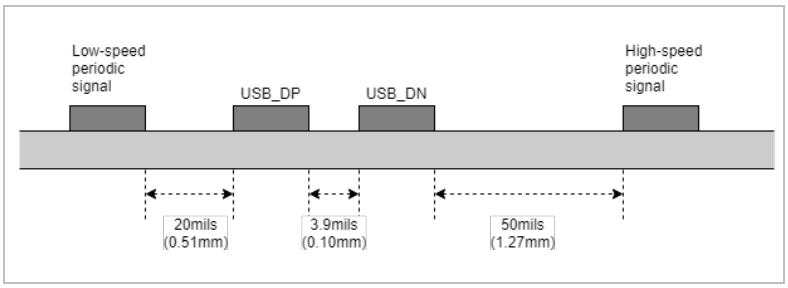


Figure 7-1 USB trace separation showing low speed signal, a differential pair and high-speed clock

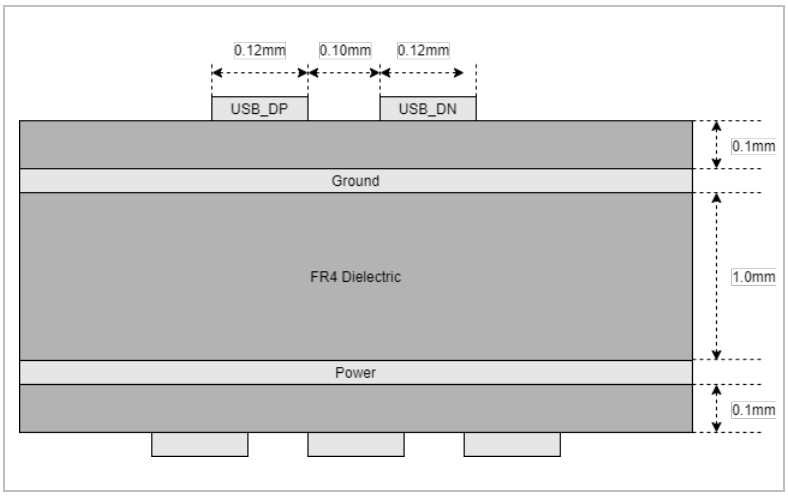


Figure 7-2 Example USB board stack

For best results, most of the routing should be done on the top layer (assuming the USB connector and XVF3510-UA are on the top layer) closest to the ground. Reference planes should be below the transmission lines in order to maintain control of the trace impedance.

It is recommended that the high-speed clock and high-speed USB differential pairs are routed first before any other routing. When routing high-speed USB signals, the following guidelines should be followed:

- High-speed differential pairs should be routed together.
- High-speed USB signal pair traces should be trace-length matched. Maximum trace-length mismatch should be no greater than 4mm.
- Ensure that high-speed signals (clocks, USB differential pairs) are routed as far away from off-board connectors as possible.
- High-speed clock and periodic signal traces that run parallel should be at least 1.27mm away from USB_DP/USB_DN (see Figure).
- Low-speed and non-periodic signal traces that run parallel should be at least 0.5mm away from USB_DP/USB_DN (see Figure).

- Route high-speed USB signals on the top of the PCB wherever possible.
- Route high-speed USB traces over continuous power planes, with no breaks. If a trade-off must be made, changing signal layers is preferable to crossing plane splits.
- Follow the 20 x h rule; keep traces 20 x h (the height above the ground plane) away from the edge of the power plane.
- Use a minimum of vias in high-speed USB traces.
- Avoid corners in the trace. Where necessary, rather than turning through a 90 degree angle, use two 45 degree turns or an arc.
- Do not route USB traces near clock sources, clocked circuits or magnetic devices.
- Avoid stubs on high speed USB signals.

7.2. JTAG AND XMOS SYSTEM DEBUG

7.2.1. JTAG MODULE

The JTAG module can be used for boundary scan testing, contact XMOS for details.

The JTAG chain structure is illustrated in the figure below.

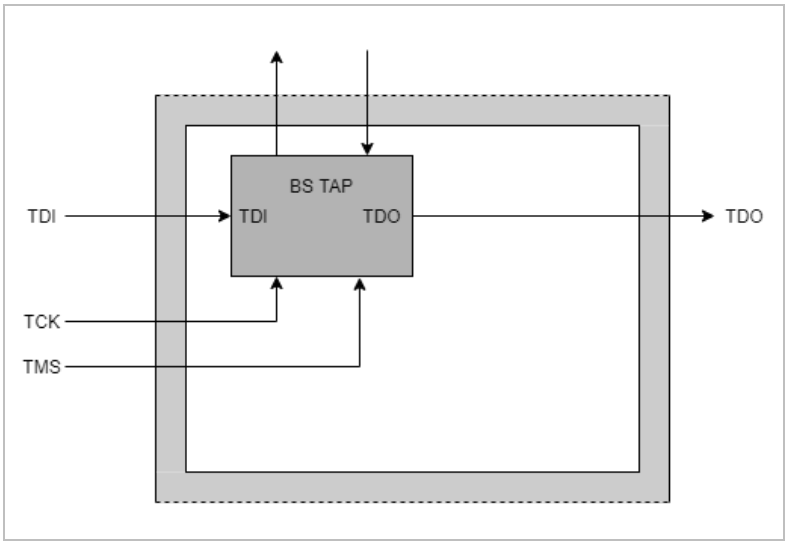


Figure 7-3 JTAG TAPs

It comprises a single IEEE 1149.1 compliant TAP that can be used for boundary scan of the I/O pins. It has a 4-bit IR and 32-bit DR. It also provides access to a chip TAP that is reserved for XMOS internal use. The JTAG module can be reset by holding TMS high for five clock cycles.

The JTAG device identification register can be read by using the IDCODE instruction. Its contents are specified in the figure below:

BIT31				DEVICE IDENTIFICATION REGISTER																BIT0
Version				Part Number														Manufacturer Identify											1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	1	1
0				0				0				0				5				6				3				3			

Figure 7-4 JTAG IDCODE

The JTAG usercode register can be read by using the USERCODE instruction. Its contents are specified in the figure below:

BIT31				USERCODE REGISTER																								BIT0			
Unused														Silicon Revision																	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0				0				0				2				8				0				0				0			

Figure 7-5 JTAG USERCODE

7.2.2. XMOS SYSTEM DEBUG CONNECTOR

For development purposes, the XTAG debugger can optionally be used to load the device firmware image. This requires the circuit board to have an XTAG header. The XTAG debug adapter has a 20-pin 0.1" female IDC header. We advise using a male IDC boxed header to guard against incorrect plug-ins. If you use a 90 degree angled header, make sure that pins 2, 4, 6, ..., 20 are along the edge of the PCB.

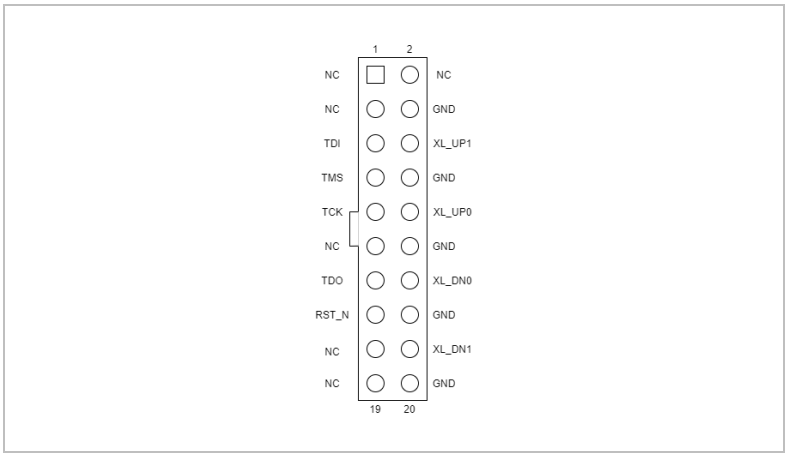


Figure 7-6 XTAG header

The XMOS Link pins (XL_UP0, XL_UP1, XL_DN0, XL_DN1) provide support for advanced XVF3510 debugging applications.

7.3. DESIGN CHECKLISTS

This section contains checklists for schematics and PCB designers using the XVF3510. Each section contains design items to check.

7.3.1. SCHEMATIC DESIGN CHECKLIST

POWER SUPPLIES

- The VDD (core) supply ramps monotonically (rises constantly) from 0V to its final value (0.95V - 1.05V) within 10ms.
- The VDD (core) supply is capable of supplying at least 700mA.
- PLL_AVDD is filtered with a low pass filter, for example, an RC filter.

POWER SUPPLY DECOUPLING

- The design has multiple decoupling capacitors per supply, for example no less than twelve, 0402 or 0603 size surface mount capacitors of 100nF in value, per supply.
- A bulk decoupling capacitor of at least 10uF is placed on each supply.

POWER-ON RESET

- The RST_N pins are asserted (low) until all supplies are good. There is enough time between VDDIO power good and RST_N to allow any boot flash to settle.

CLOCKS

- The CLK input pin is supplied with a clock with monotonic rising edges and low jitter.
- A 24MHz reference clock must be connected to the CLK pin for all implementations.
- MCLK_INOUT is connected to MCLK_IN via a PCB trace outside the device.
- All clock signals (CLK, MIC_CLK, QSPI_CLK, SPI_CLK, MCLK_IN, MCLK_INOUT, BCLK, LRCLK) and other audio signals must be routed following high speed digital design guidelines, and may need buffering.

BOOT

- To boot from QSPI flash, QSPI_CS_N, QSPI_D0, QSPI_D1/BOOTSEL, QSPI_D2, QSPI_D3, QSPI_CLK/SPI_CLK are connected to the flash device.
- To boot from the local host processor through SPI, QSPI_D1/BOOTSEL must be pulled high and QSPI_CLK/SPI_CLK, SPI_CS_N, SPI_MOSI and SPI_MISO must be connected to the host processor.

MICROPHONES

- Both MIC_DATA pins are connected together
- The two PDM Microphones should be set to output on alternating edges of the MIC_CLK signal. Left microphone on rising edge and Right microphone on falling edge.

JTAG AND DEBUGGING

- It is recommended that XSYS connection is always incorporated, for debug purposes, even if the header is not used.
- If no XSYS header is used, ensure there is a method to program the SPI-flash device

7.3.2. PCB LAYOUT DESIGN CHECKLIST

GROUND PLANE

- Multiple vias (e.g. minimum of 10 evenly spaced) have been used to connect the ground paddle to the PCB ground plane. These minimise impedance and conduct heat away from the device.
- Except for ground vias, ensure there are no (or only a few) vias underneath or closely around the device to create a good, solid, ground plane.

POWER SUPPLY DECOUPLING

- A decoupling capacitor is placed close to each supply pin.
- The ground side of each decoupling capacitor has a direct path back to the central ground pad of the device.

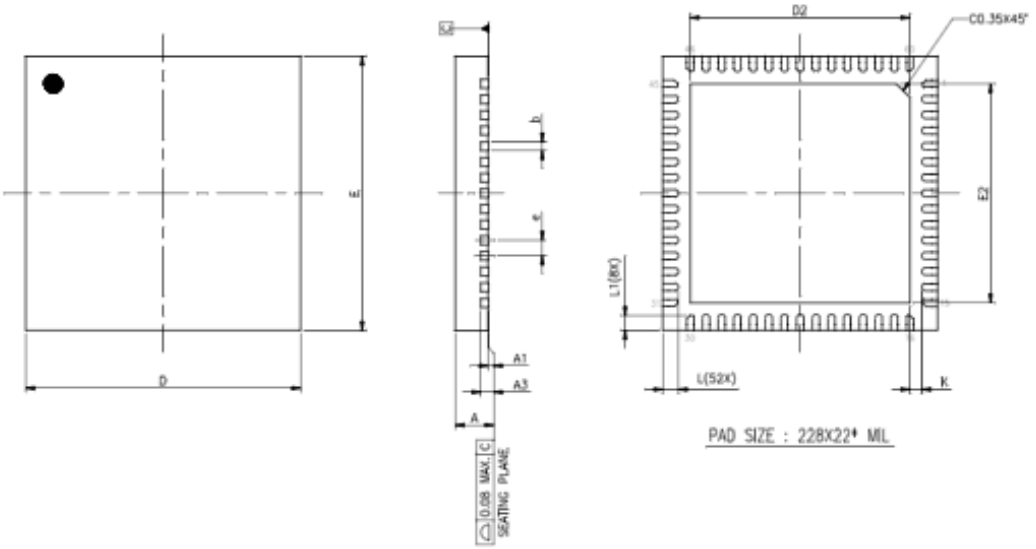
PLL_AVDD SUPPLY

- Ensure the PLL_AVDD filter is placed close to the PLL_AVDD pin.

8. PACKAGE INFORMATION

8.1. PACKAGE DIMENSIONS

The XVF3510 uses a 60 pin Quad Flat No-leads package (QFN) on a 0.4mm pin-pitch with an exposed ground paddle/heat slug. The land patterns and solder stencils will depend on the PCB manufacturing process. We recommend you refer to the IPC specification for development of land patterns. This standard aims to achieve desired targets of heel, toe and side fillets for solder-joints.

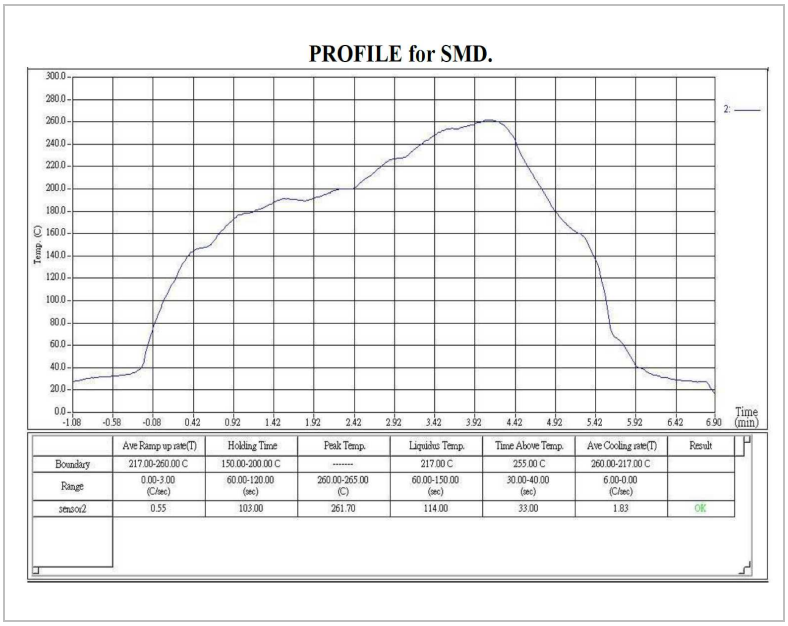


SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
D	6.90	7.00	7.10
E	6.90	7.00	7.10
e		0.40 BSC	
K	0.20	—	—
b	0.15	0.20	0.25
D2	5.50	5.60	5.70
E2	5.50	5.60	5.70
L1	0.33	0.38	0.43
L	0.35	0.40	0.45

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

Figure 8-1 QFN60 package dimensions

8.2. REFLOW PROFILE



	Ave Ramp up rate(T)	Holding Time	Peak Temp.	Liquidus Temp.	Time Above Temp.	Ave Cooling rate(T)	Result
Boundary	217.00-260.00 C	150.00-200.00 C	-------	217.00 C	255.00 C	260.00-217.00 C	
Range	0.00-3.00 (C/sec)	60.00-120.00 (sec)	260.00-265.00 (C)	60.00-150.00 (sec)	30.00-40.00 (sec)	6.00-0.00 (C/sec)	
sensor2	0.55	103.00	261.70	114.00	33.00	1.83	OK

8.3. DEVICE MARKINGS

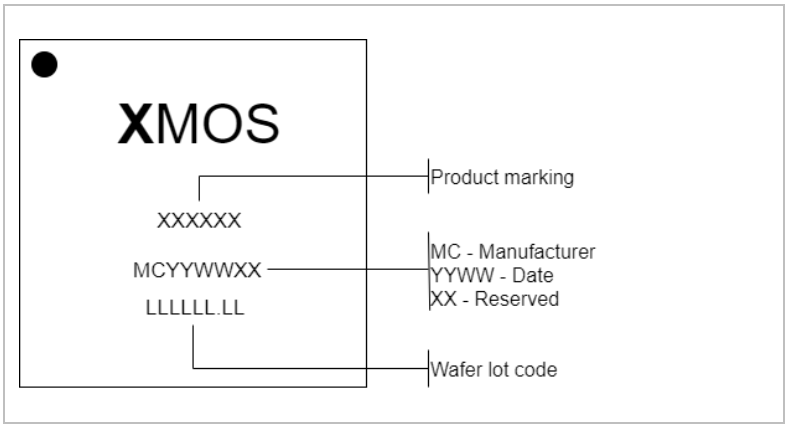


Figure 8-2 Part marking scheme

8.4. THERMAL CHARACTERISTICS

Table 8-1 Junction temperature

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
Tj	Junction temperature	-	-	125	°C	

Table 8-2 Package thermal parameters

SYMBOL	PARAMETER	0M/S AIR SPEED	1M/S AIR SPEED	2M/S AIR SPEED	UNITS	NOTES
θJA	Junction to Ambient thermal resistance	25.2	21.4	20.1	°C/W	A, B
θJB	Junction to Board thermal resistance	4.1	4.1	4.1	°C/W	A, B
θJC	Junction to Package Top thermal resistance	9.7	9.7	9.7	°C/W	A, B
ΨJT	Junction to Package Top thermal characterisation parameter	0.09	0.3	0.4	°C/W	A, C
ΨJB	Junction to Board thermal characterisation parameter	5.0	4.9	4.9	°C/W	A, C

A: Thermal modelling based on 4 layer PCB and 55°C ambient temperature.

B: Values of θJA, θJB and θJC are provided for PCB design considerations.

C: Refer to JESD51-12, *Guidelines for Reporting and Using Package Thermal Information,* for further information on Thermal Characterisation Parameters and their usage.

9. FURTHER INFORMATION

9.1. DOCUMENTATION

Table 9-1 Additional documentation

DOCUMENT TITLE	DOWNLOAD
XVF3510 User Guide	https://www.xmos.ai/file/xvf3510-user-guide
XMOS xTIMEcomposer Tools User Guide	https://www.xmos.ai/file/tools-user-guide
XVF3510 Development Kit Setup Guide	https://www.xmos.ai/file/xvf3510-dev-kit-setup-guides

9.2. DEVICE FIRMWARE AND DRIVERS

Table 9-2 Device firmware

DEVICE FIRMWARE & APPLICATION SOFTWARE	DOWNLOAD
XVF3510 firmware and Sample Host control applications	https://www.xmos.ai/file/xvf3510-ua-release
xTIMEcomposer Programming Tools	https://www.xmos.ai/software-tools

9.3. PART ORDERING

Table 9-3 Ordering codes

PRODUCT CODE	MARKING	QUALIFICATION
XVF3510-QF60-C	VSM06C	Commercial

10. REVISION HISTORY

DOCUMENT VERSION	RELEASE DATE	CHANGE DESCRIPTION
XM-014165-PC-4	23 Jul 2020	Updated for V4.0 release – Replaces XM-013898-PC
XM-014165-PC-5	18 Sept 2020	V4.1 firmware adds USB host volume control block