xCORE Microphone Array Hardware Manual

IN THIS DOCUMENT

xCORE Microphone Array evaluation board is an application specific design targeted at microphone aggregation and array microphones used Voice User Interface (VUI) applications. It integrates all the necessary building blocks including:

- multiple omni-directional microphones
- on-board low-jitter clock sources
- configurable user input buttons
- ethernet, USB2.0 device and/or I2S/I2C host connectivity

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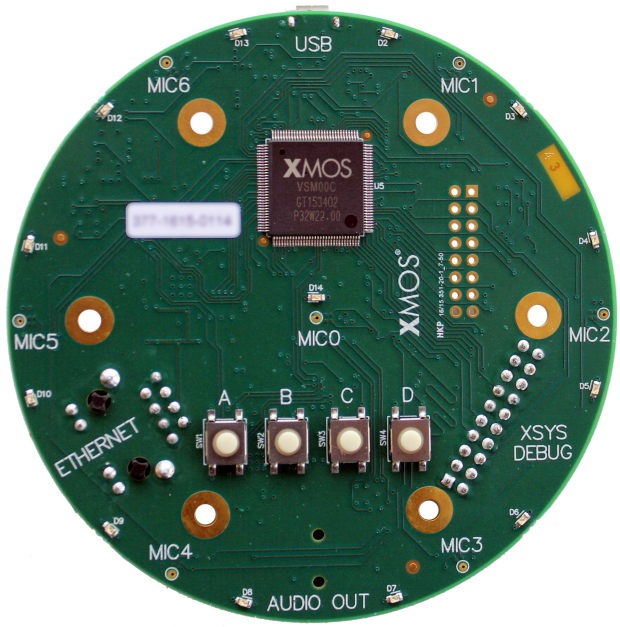

Figure 1: xCORE Microphone Array evaluation board - top

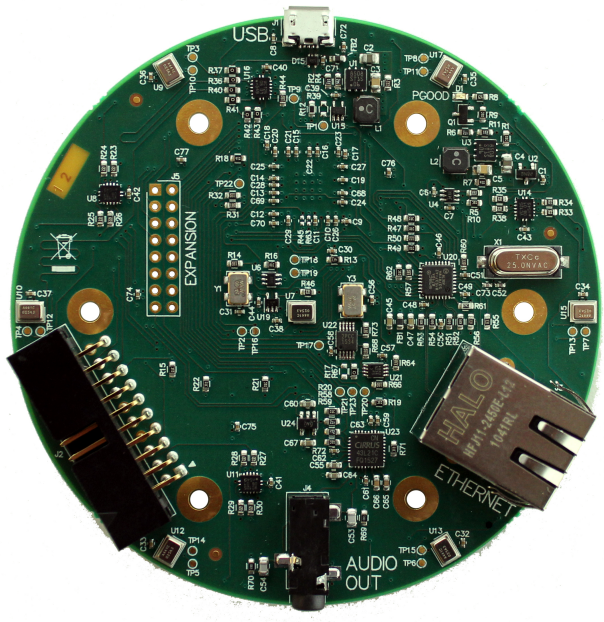

Figure 2: xCORE Microphone Array evaluation board - bottom

1 Features

The xCORE Microphone Array block diagram is shown below. It includes:

- xCORE-200 (XUF216-512-TQ128) multicore microcontroller device
- Seven AKUSTICA AKU441 MEMS microphones
- A micro-USB connector for USB2.0 device connectivity and power
- An RJ45 connector for 10/100Mbps Ethernet connectivity
- An expansion header for I2S, I2C and/or other connectivity and control solutions
- Four general purpose push-button switches
- 12 user-controlled LEDs
- Low-jitter clock source
- An xSYS connector for an xTAG debug adapter

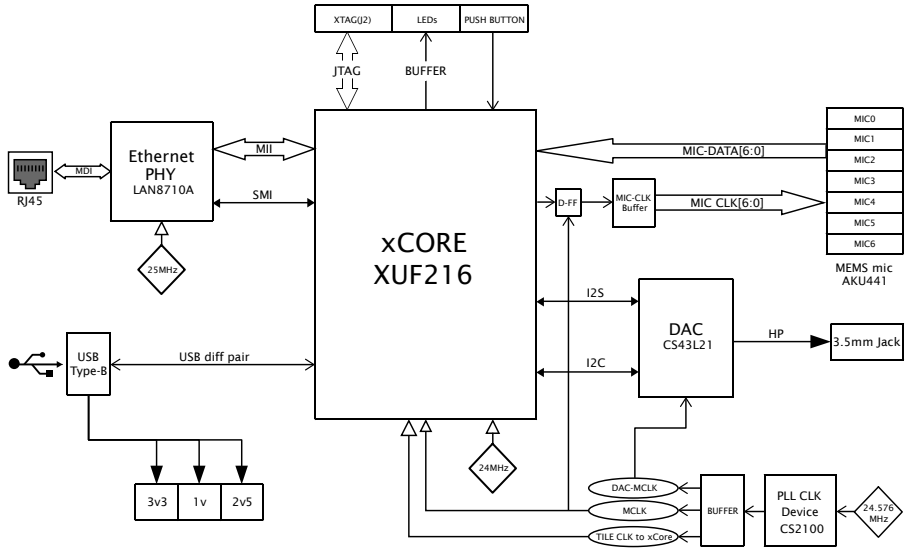

Figure 3: xCORE Microphone Array block diagram

2 Introduction

The xCORE Microphone Array evaluation board is based on a two-tile xCORE-200 XUF216-512-TQ128 device, which contains 16 32-bit logical processing cores that deliver up to 2000 MIPS compute and integrates 2MBytes Quad Serial Peripheral Interface (QSPI) flash.

For general information on xCORE-200 devices see the xCORE-200 Architecture Overview[1]. For device specific information on the XUF216-512-TQ128 device see XUF216-512-TQ128 Datasheet[2].

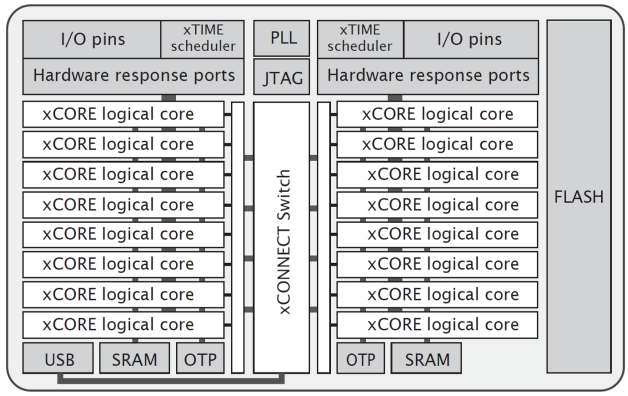

Figure 4: xCORE-200 XUF216-512-TQ128 device

3 Clock sources and distribution

The board includes three clock sources:

- xCORE-200 reference clock - 24MHz oscillator (Y1)
- Ethernet PHY reference clock - 25MHz crystal (X1)
- Low jitter clock source - 24.576MHz oscillator, used as reference clock to the CS2100-CP (CirrusLogic) Fractional-N PLL (U22).

  The CS2100 generates a low-jitter output signal that is distributed to the xCORE-200 device (Tile1 & MCLK) and DAC (MIC-CLK). The CS2100 device is configured using the I2C interface.

[1] http://www.xmos.com/published/xcore-architecture
[2] http://www.xmos.com/published/xuf216-512-tq128-datasheet?version=latest

4 Stereo DAC with headphone amplifier

A CS43L21 stereo DAC with integrated headphone amplifier is used to generate audio output on a 3.5mm audio jack. The CS43L21 is connected to the xCORE-200 through an I2S interface and is configured using an I2C interface.

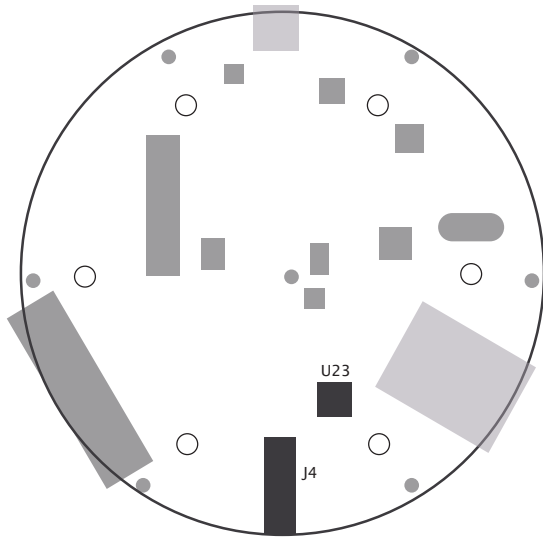

Figure 5: Stereo DAC/HPA components

The CS43L21 stereo DAC/HPA device is configured using the I2C bus.

Pin	Port	Signal
X1D26	P4E0	I2C_SCL
X1D27	P4E1	I2C_SDA
X1D28	P4F0	DAC_RST_N
X1D36	P1M0	I2S_BCLK
X1D37	P1N0	I2S_LRCLK
X1D39	P1P0	I2S_DAC_DATA

The addresses of the CS2100-CP and CS43L21 devices on the I2C bus are shown below.

Device	Ref ID	Address	
CS2100-CP	U22	0b1001110	0x4E
CS43L21	U23	0b1001010	0x4A

5 MEMS Microphones

The AKU441 MEMS microphones used in this evalution board have a bottom port and measure 4mmx3mmx1mm, suitable for voice interface applications.

One microphone is placed at the center of the board (MIC_0). The remaining six microphones are distributed equidistant around the board edge.

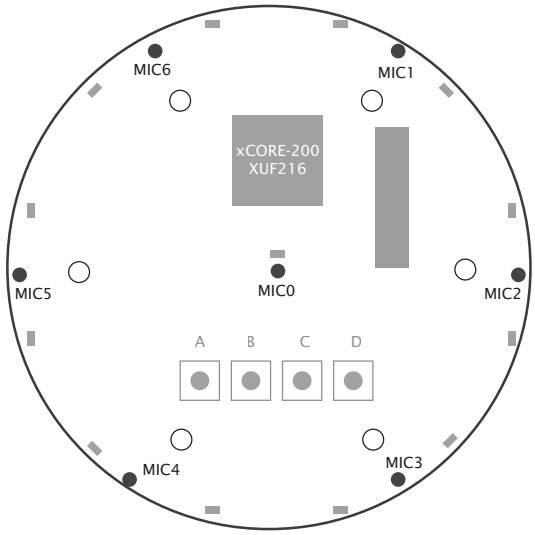

Figure 6: MEMS microphones

The microphone signals are mapped onto the xCORE-200 device as show in Figure 7:

Microphone	xCORE GPIO	Port
MIC_CLK	X0D12	P1E0
MIC_0	X0D14	P4C0
MIC_1	X0D15	P4C1
MIC_2	X0D16	P4D0
MIC_3	X0D17	P4D1
MIC_4	X0D18	P4D2
MIC_5	X0D19	P4D3
MIC_6	X0D20	P4C2

Figure 7: MEMS microphone xCORE GPIO

6 Ethernet Connectivity

10/100 Mbps Ethernet connectivity consists of Microchip LAN8710A Ethernet PHY (U20) and an RJ45 connector (J3) with integrated magnetics. The PHY uses the 25MHz crystal as a reference clock.

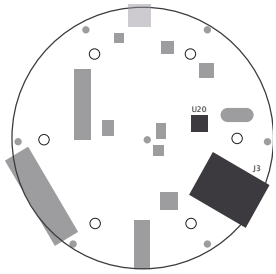

Figure 8: Ethernet components

The MII signals are mapped onto the xCORE-200 device as shown in Figure 9:

RGMII signal	xCORE GPIO	Port
RX_CLK	X1D00	P1A0
TX_CLK	X1D01	P1B0
RX0	X1D02	P4A0
RX1	X1D03	P4A1
RX2	X1D08	P4A2
RX3	X1D09	P4A3
TX0	X1D04	P4B0
TX1	X1D05	P4B1
TX2	X1D06	P4B2
TX3	X1D07	P4B3
RXDV	X1D10	P1C0
TXEN	X1D11	P1D0
MDC	X1D14	P4C0
MDIO	X1D15	P4C1
ETH_RST_N	X1D29	P4F1
RXER	X1D35	P1L0

Figure 9: Ethernet xCORE GPIO

7 General purpose user interface

The board has 13 LEDs that are controlled by the xCORE-200 GPIO.

LED_0 - LED_11 (D2-D13) are positioned around the edge of the board, one each side of every microphone. LED_12 (D14) is positioned next to the middle microphone.

A green LED (PGOOD) by the USB connector indicates a 3V3 power good signal.

Four general purpose push-button switches are provided. When pressed, each button creates a connection from the I/O to GND. To ensure correct behaviour, the port connected to the buttons (P4A) must always be defined as an input.

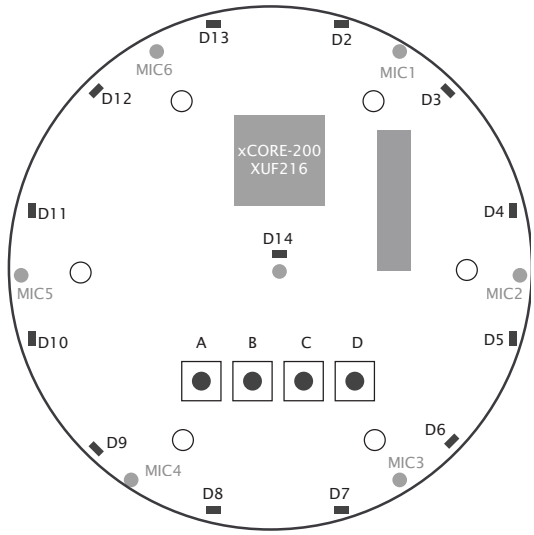

Figure 10: General purpose user interface components

The signal mapping of the user interface components is shown in Figure 11

UI signal	xCORE GPIO	Port
LED_0	X0D26	P4E0
LED_1	X0D27	P4E1
LED_2	X0D28	P4F0
LED_3	X0D29	P4F1
LED_4	X0D30	P4F2
LED_5	X0D31	P4F3
LED_6	X0D32	P4E2
LED_7	X0D33	P4E3
LED_8	X0D43	P1K0
LED_9	X0D35	P1L0
LED_10	X0D36	P1M0
LED_11	X0D37	P1N0
LED_12	X0D38	P1O0
BUTTON_A	X0D02	P4A0
BUTTON_B	X0D03	P4A1
BUTTON_C	X0D08	P4A2
BUTTON_D	X0D09	P4A3

Figure 11: User interface GPIO

The LED output must be set low to light the corresponding LED.

8 Expansion Header

The board has an expansion header containing 7 general purpose IOs, controlled by the xCORE-200, and an audio MCLK.

By removing R67 and inserting a 0R link into R17, the expansion header audio MCLK can be used as an alternative to the CS2100-CP (CirrusLogic) Fractional-N PLL (U22) output.

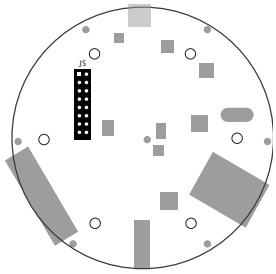

Figure 12: Expansion header location

The signal mapping of the expansion header is shown in Figure 13

Header pin	xCORE GPIO	Port
1	X0D22	P1G0
2	GND	
3	X0D23	P1H0
4	GND	
5	X0D00	P1A0
6	GND	
7	X0D11	P1D0
8	GND	
9	X0D24	P1I0
10	X0D39	P1P0
11	GND	
12	X0D25	P1J0
13	3V3	
14	GND	
15	EXT_MCLK	
16	GND	

Figure 13: Expansion header GPIO

9 USB Port

The USB Micro-B receptacle (J1) is connected to the USB PHY integrated in the XUF216 device, and provides power for the on-board circuits, and USB interface connectivity. Voltage tolerance should be as per USB VBUS specification values.

The power source is used to generate the following voltage rails:

- +1V0 (Core voltage to XMOS device)
- +2v5 (for headphone amplifier in DAC device)
- +3v3 for GPIOs and other accessory devices

Proper power-on sequence is indicated by power good LED (D1) in bottom side of the board.

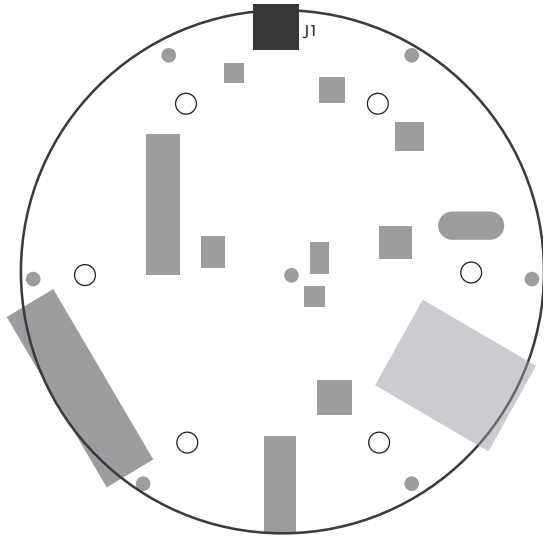

Figure 14: USB components

NOTE: J1 must be connected at all times to provide power to the board.

NOTE: as this board is self-powered, the USB_VBUS pin on U5 is not connected. To ensure that the USB Audio 2.0 reference software operates correctly with this board, please refer to the following design advisory:

http://www.xmos.com/doc/XM-012350-DA

10 Flash Memory

The XUF216-512-TQ128 device includes 2MBytes of QSPI flash memory, which is interfaced by the GPIO connections shown in Figure 15:

QSPI connection	Pin	Port
QSPI_SS	X0D01	P1B
QSP_D0	X0D04	P4B0
QSP_D1	X0D05	P4B1
QSP_D2	X0D06	P4B2
QSP_D3	X0D07	P4B3
SPI_CLK	X0D10	P1C

Figure 15: QSPI Flash

11 xSYS connector

A standard XMOS xSYS interface (J2) is provided to allow host debug of the board via JTAG.

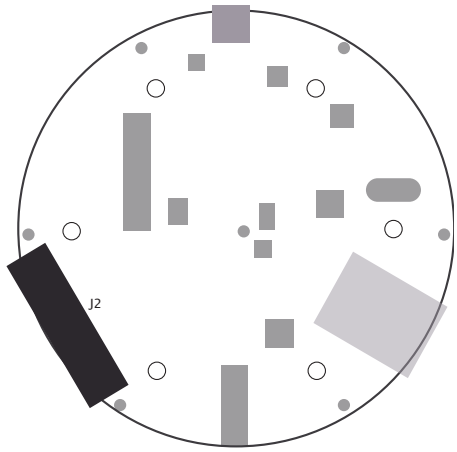

Figure 16: xsYS connector

XSYS signal	xCORE GPIO	Header pin	Description
TMS	See note	7	JTAG Test Mode Select
TCK	See note	9	JTAG Test Clock
TDI	See note	5	JTAG Test Data In - from debug adapter to xCORE
TDO	See note	13	JTAG Test Data Out - from xCORE to debug adapter
RST_N	See note	15	System Reset - active low, resets xCORE device
GND		4, 8, 12, 16, 20	Ground
XL_UP1	X0D43	6	XMOS link, uplink bit 1
XL_UP0	X0D42	10	XMOS link, uplink bit 0
XL_DN1	X0D40	14	XMOS link, downlink bit 1
XL_DN0	X0D41	18	XMOS link, downlink bit 0

Figure 17: XSYS Connector Pinout

Notes:

- JTAG connections occupy dedicated connections

12 xCORE Microphone Array Portmap

The table below provides a full description of the port-pin mappings described throughout this document for the xCORE Microphone Array board.

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X0D00	$1A^0$					
X0D01	$1B^0$					QSPI_CS
X0D02		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	BUTTON_A
X0D03		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	BUTTON_B
X0D04		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	QSPI_D0
X0D05		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	QSPI_D1
X0D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	QSPI_D2
X0D07		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	QSPI_D3
X0D08		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	BUTTON_C
X0D09		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	BUTTON_D
X0D10	$1C^0$					QSPI_CLK
X0D11	$1D^0$					
X0D12	$1E^0$					MIC_CLK
X0D13	$1F^0$					MCLK_XCORE
X0D14		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	MIC_0_DATA
X0D15		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	MIC_1_DATA
X0D16		$4D^0$	$8B^2$	$16A^{10}$		MIC_2_DATA
X0D17		$4D^1$	$8B^3$	$16A^{11}$		MIC_3_DATA
X0D18		$4D^2$	$8B^4$	$16A^{12}$		MIC_4_DATA
X0D19		$4D^3$	$8B^5$	$16A^{13}$		MIC_5_DATA
X0D20		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	MIC_6_DATA
X0D21		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	
X0D22	$1G^0$					
X0D23	$1H^0$					
X0D24	$1I^0$					
X0D25	$1J^0$					
X0D26		$4E^0$	$8C^0$	$16B^0$		LED_0
X0D27		$4E^1$	$8C^1$	$16B^1$		LED_1
X0D28		$4F^0$	$8C^2$	$16B^2$		LED_2
X0D29		$4F^1$	$8C^3$	$16B^3$		LED_3
X0D30		$4F^2$	$8C^4$	$16B^4$		LED_4
X0D31		$4F^3$	$8C^5$	$16B^5$		LED_5
X0D32		$4E^2$	$8C^6$	$16B^6$		LED_6
X0D33		$4E^3$	$8C^7$	$16B^7$		LED_7
X0D34	$1K^0$					LED_8
X0D35	$1L^0$					LED_9
X0D36	$1M^0$		$8D^0$	$16B^8$		LED_10
X0D37	$1N^0$		$8D^1$	$16B^9$		LED_11
X0D38	$1O^0$		$8D^2$	$16B^{10}$		LED_12
X0D39	$1P^0$		$8D^3$	$16B^{11}$		LED_OEN
X0D40			$8D^4$	$16B^{12}$		XL_DN1
X0D41			$8D^5$	$16B^{13}$		XL_DN0
X0D42			$8D^6$	$16B^{14}$		XL_UP0
X0D43			$8D^7$	$16B^{15}$		XL_UP1

Figure 18: xCORE Microphone Array Portmap: Tile 0

Pin	1-bit	4-bit	8-bit	16-bit	32-bit	Signal
X1D00	$1A^0$					ETH_RXCLK
X1D01	$1B^0$					ETH_TXCLK
X1D02		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$	ETH_RXD_0
X1D03		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$	ETH_RXD_1
X1D04		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$	ETH_TXD_0
X1D05		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$	ETH_TXD_1
X1D06		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$	ETH_TXD_2
X1D07		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$	ETH_TXD_3
X1D08		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$	ETH_RXD_2
X1D09		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$	ETH_RXD_3
X1D10	$1C^0$					ETH_RXDV
X1D11	$1D^0$					ETH_TXEN
X1D14		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$	ETH_MDC
X1D15		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$	ETH_MDIO
X1D16		$4D^0$	$8B^2$	$16A^{10}$		PLL_SYNC
X1D17		$4D^1$	$8B^3$	$16A^{11}$		
X1D18		$4D^2$	$8B^4$	$16A^{12}$		
X1D19		$4D^3$	$8B^5$	$16A^{13}$		
X1D20		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$	
X1D21		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$	
X1D26		$4E^0$	$8C^0$	$16B^0$		I2C_SCLK
X1D27		$4E^1$	$8C^1$	$16B^1$		I2C_SDA
X1D28		$4F^0$	$8C^2$	$16B^2$		DAC_RST_N
X1D29		$4F^1$	$8C^3$	$16B^3$		ETH_RST_N
X1D30		$4F^2$	$8C^4$	$16B^4$		
X1D31		$4F^3$	$8C^5$	$16B^5$		
X1D32		$4E^2$	$8C^6$	$16B^6$		
X1D33		$4E^3$	$8C^7$	$16B^7$		
X1D35	$1L^0$					ETH_RX_ERR
X1D36	$1M^0$		$8D^0$	$16B^8$		I2S_BCLK
X1D37	$1N^0$		$8D^1$	$16B^9$		I2S_LRCLK
X1D38	$1O^0$		$8D^2$	$16B^{10}$		MCLK_TILE1
X1D39	$1P^0$		$8D^3$	$16B^{11}$		I2S_DAC_DATA
X1D40			$8D^4$	$16B^{12}$		
X1D41			$8D^5$	$16B^{13}$		
X1D42			$8D^6$	$16B^{14}$		
X1D43			$8D^7$	$16B^{15}$		

Figure 19: xCORE Microphone Array Portmap: Tile 1

13 Operating requirements

A USB 2.0 high-speed compliant cable of less than 3m in length should be used when operating the xCORE Microphone Array board. XMOS cannot guarantee correct operation of the xCORE Microphone Array board should any other cable be used.

This product is, like most electronic equipment, sensitive to Electrostatic Discharge (ESD) events. Users should operate the xCORE Microphone Array board with appropriate ESD precautions in place.

14 Dimensions

This xCORE Microphone Array board has diameter of 90 mm and board thickness of 1.6mm.

15 RoHS and REACH

The xCORE Microphone Array board complies with appropriate RoHS2 and REACH regulations and is a Pb-free product.

The xCORE Microphone Array board is subject to the European Union WEEE directive and should not be disposed of in household waste. Alternative requirements may apply outside of the EU.

16 Schematics

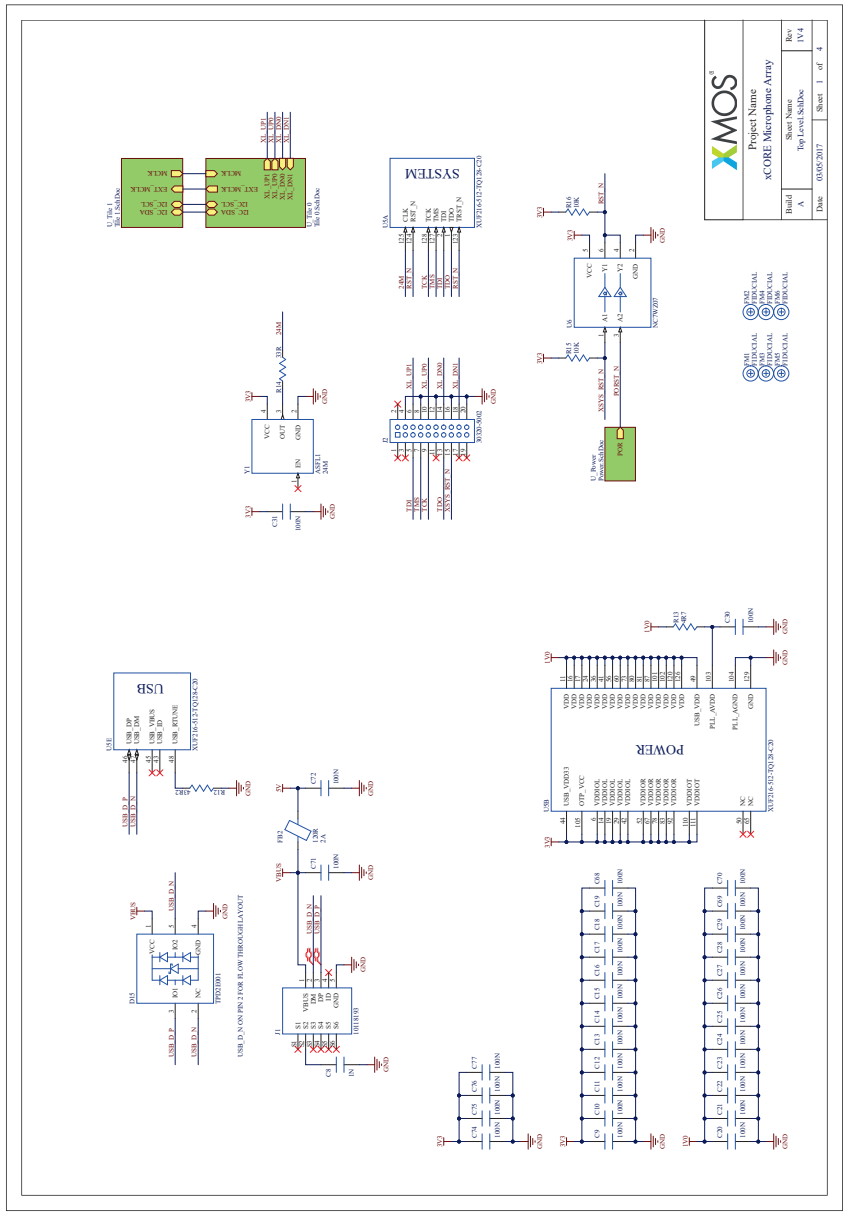

Figure 20: xCORE Microphone Array board - Power entry and xCORE-200 Configuration

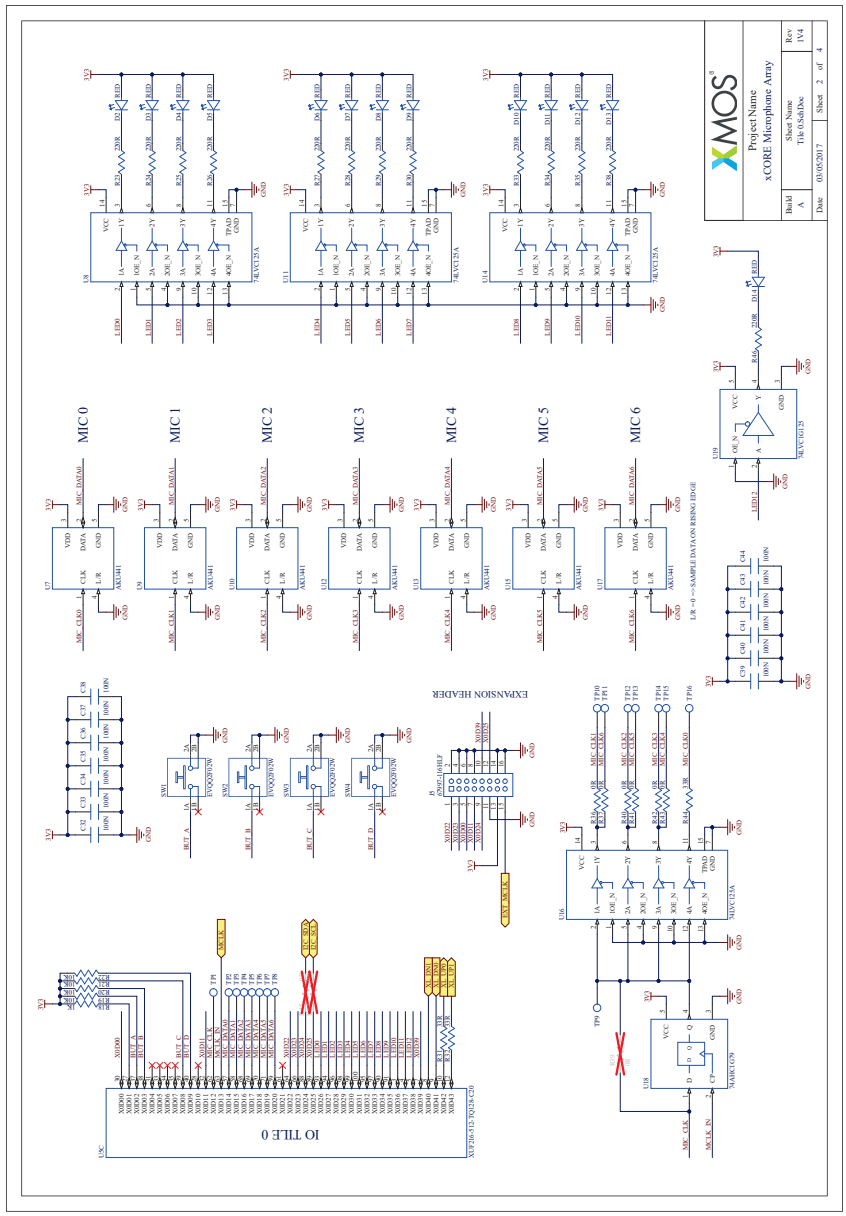

Figure 21: xCORE Microphone Array board - Microphone

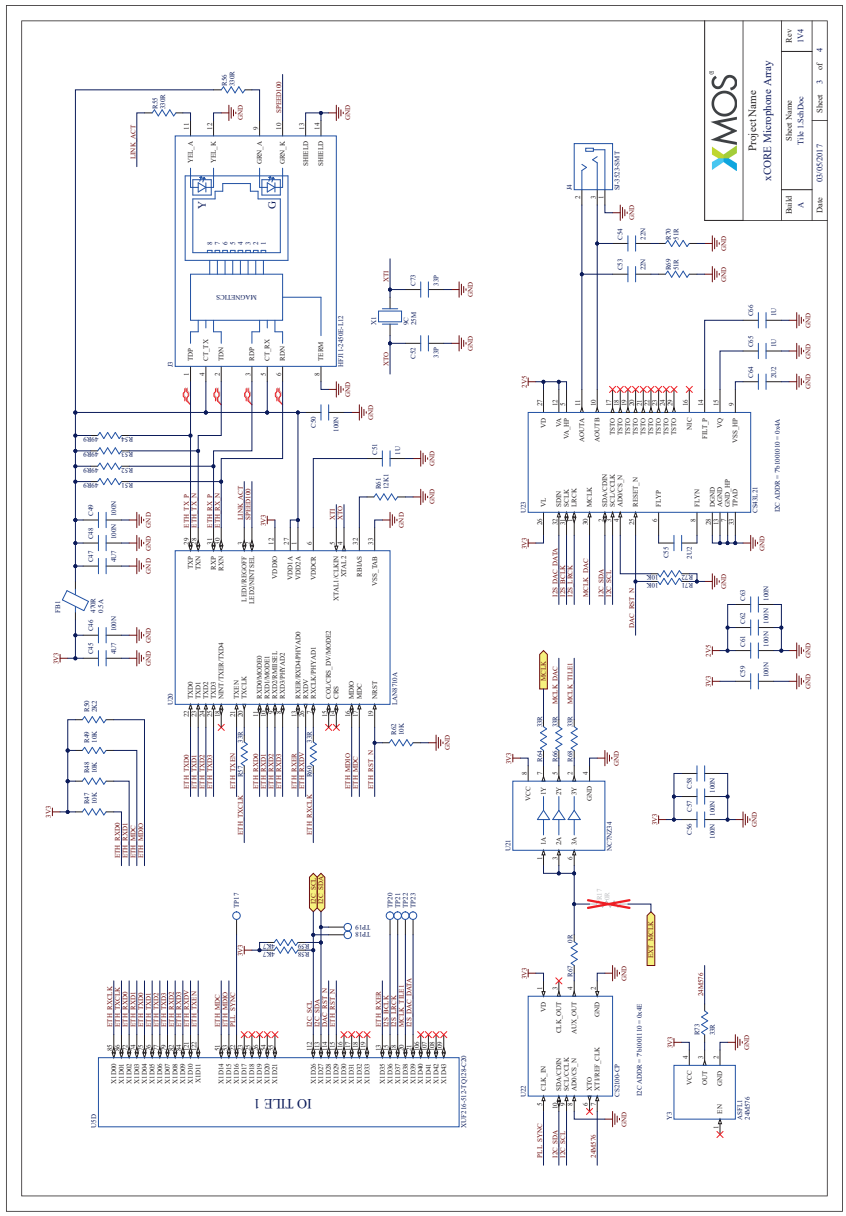

Figure 22: xCORE Microphone Array board - Ethernet and Stereo DAC with Headphone Jack circuitry

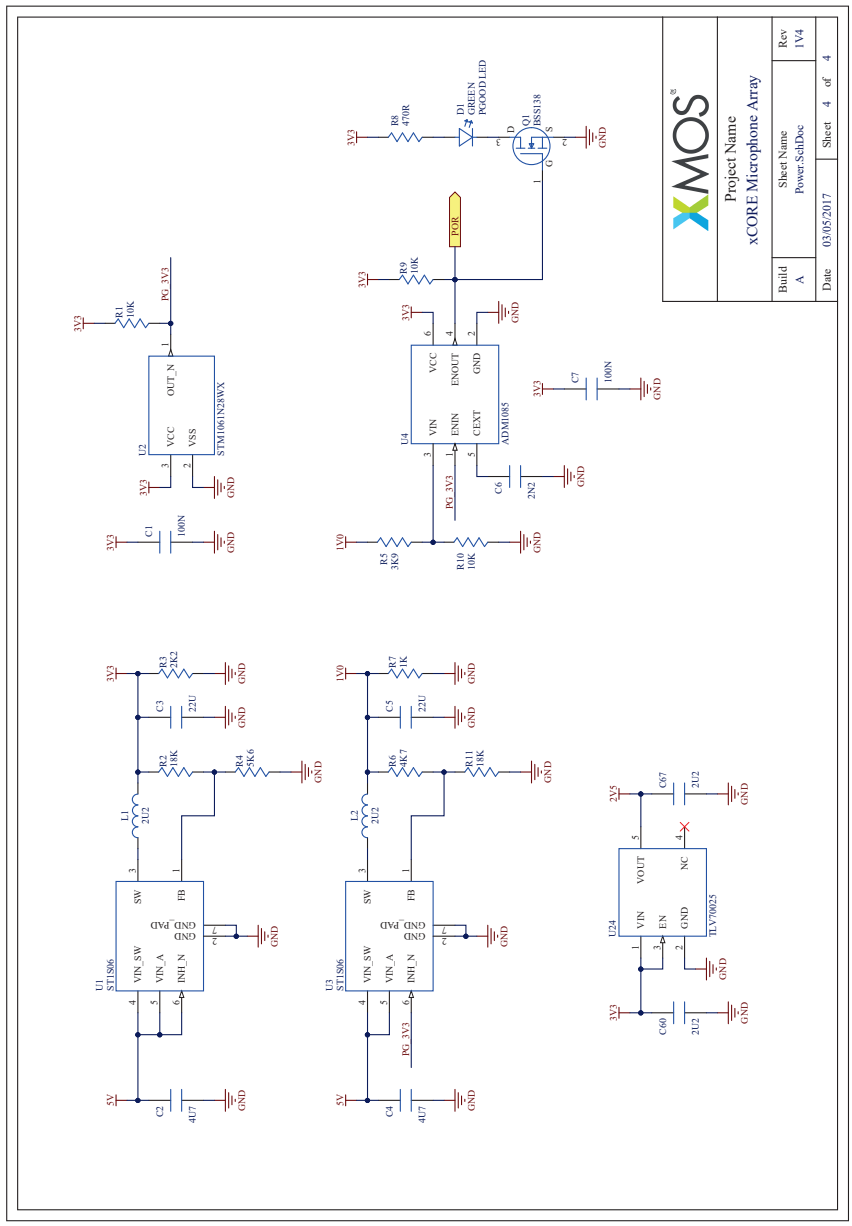

Figure 23: xCORE Microphone Array board - Voltage rail LDOs and reset circuit

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