SPI Library

A software defined, industry-standard, SPI (serial peripheral interface) component that allows you to control an SPI bus via the xCORE GPIO hardware-response ports. SPI is a four-wire hardware bi-directional serial interface.

The SPI bus can be used by multiple tasks within the xCORE device and (each addressing the same or different slaves) and is compatible with other slave devices on the same bus.

Features

- SPI master and SPI slave modes.
- Supports speed of up to 100 Mbit.
- Multiple slave device support
- All clock polarity and phase configurations supported.

Typical Resource Usage

This following table shows typical resource usage in some different configurations. Exact resource usage will depend on the particular use of the library by the application.

Configuration	Pins	Ports	Clocks	Ram	Logical cores
Master (synchronous, zero clock blocks)	4	4 (1-bit)	0	~1.3K	0
Master (synchronous, one clock block)	4	4 (1-bit)	1	~2.7K	0
Master (asynchronous)	4	4 (1-bit)	2	~3.3K	≤ 1
Slave (32 bit transfer mode)	4	4 (1-bit)	1	~0.8K	≤ 1
Slave (8 bit transfer mode)	4	4 (1-bit)	1	~0.8K	≤ 1

The number of pins is reduced if either of the data lines are not required.

Software version and dependencies

This document pertains to version 3.0.2 of this library. It is known to work on version 14.1.1 of the xTIMEcomposer tools suite, it may work on other versions.

The library does not have any dependencies (i.e. it does not rely on any other libraries).

Related application notes

The following application notes use this library:

- AN00160 - How to communicate as SPI master
- AN00161 - How to communicate as SPI slave