SDRAM Library

The XMOS SDRAM module is designed for 16 bit read and write access of arbitrary length at up to 62.5MHz clock rates. It uses an optimized pinout with address and data lines overlaid along with other pinout optimizations to implement 16 bit read/write with up to 13 address lines with a total of just 20 pins.

Features

The SDRAM component has the following features:

- Configurability of:
  - SDRAM geometry
  - clock rate
  - refresh properties
- Supports:
  - read
  - write
  - one or more clients
  - asynchronous command decoupling with a command queue of length 8 for each client
  - refresh handled by the SDRAM component itself
- Requires a single core for the server

Components

- SDRAM server
- Memory address allocator

Resource Usage

This following table shows typical resource usage in some different configurations. Exact resource usage will depend on the particular use of the library by the application.

Configuration	Pins	Ports	Clocks	Ram	Logical cores
SDRAM server	20	4 (1-bit), 1 (16-bit)	1	~4.0K	1
Memory address allocator	0	0	0	~0.2K	0

Software version and dependencies

This document pertains to version 3.0.2 of this library. It is known to work on version 14.1.1 of the xTIMEcomposer tools suite, it may work on other versions.

The library does not have any dependencies (i.e. it does not rely on any other libraries).

Related application notes

The following application notes use this library:

- AN00170 - Using the SDRAM library