XS1 port-to-pin mapping

On XS1 devices, pins are used to interface with external components via ports and to construct links to other devices over which channels are established. The ports are multiplexed, allowing the pins to be configured for use by ports of different widths. Figure 1 gives the XS1 port-to-pin mapping, which is interpreted as follows:

- The name of each pin is given in the format X*n*D*pq* where *n* is a valid xCORE Tile number for the device and *pq* exists in the table. The physical position of the pin depends on the packaging and is given in the device datasheet.
- Each link is identified by a letter A-D. The wires of a link are identified by means of a superscripted digit 0-4.
- Each port is identified by its width (the first number 1, 4, 8, 16 or 32) and a letter that distinguishes multiple ports of the same width (A-P). These names correspond to port identifiers in the header file `<xs1.h>` (for example port 1A corresponds to the identifier `XS1_PORT_1A`). The individual bits of the port are identified by means of a superscripted digit 0-31.
- The table is divided into six rows (or *banks*). The first four banks provide a selection of 1, 4 and 8-bit ports, with the last two banks enabling the single 32-bit port. Different packaging options may export different numbers of banks; the 16-bit and 32-bit ports are not available on small devices.

The ports used by a program are determined by the set of XC port declarations. For example, the declaration

```
on tile [0] : in port p = XS1_PORT_1A
```

uses the 1-bit port 1A on xCORE Tile 0, which is connected to pin X0D00.

Usually the designer should ensure that there is no overlap between the pins of the declared ports, but the precedence has been designed so that, if required, portions of the wider ports can be used when overlapping narrower ports are used. The ports to the left of the table have precedence over ports to the right. If two ports are declared that share the same pin, the narrower port takes priority. For example:

```
on tile[2] : out port p1 = XS1_PORT_32A;
on tile[2] : out port p2 = XS1_PORT_8B;
on tile[2] : out port p3 = XS1_PORT_4C;
```

In this example:

- I/O on port `p1` uses pins X2D02 to X2D09 and X2D49 to X2D70.
- I/O on port `p2` uses pins X2D16 to X2D19; inputting from `p2` results in undefined values in bits 0, 1, 6 and 7.
- I/O on port `p3` uses pins X2D14, X2D15, X2D20 and X2D21; inputting from `p1` results in undefined values in bits 28-31, and when outputting these bits are not driven.

Figure 1: Available ports and links for each pin

	⇐ highest		Precedence			lowest ⇒
Pin	link	1-bit ports	4-bit ports	8-bit ports	16-bit ports	32-bit port
XnD00		$1A$				
XnD01	A^4 out	$1B$				
XnD02	A^3 out		$4A^0$	$8A^0$	$16A^0$	$32A^{20}$
XnD03	A^2 out		$4A^1$	$8A^1$	$16A^1$	$32A^{21}$
XnD04	A^1 out		$4B^0$	$8A^2$	$16A^2$	$32A^{22}$
XnD05	A^0 out		$4B^1$	$8A^3$	$16A^3$	$32A^{23}$
XnD06	A^0 in		$4B^2$	$8A^4$	$16A^4$	$32A^{24}$
XnD07	A^1 in		$4B^3$	$8A^5$	$16A^5$	$32A^{25}$
XnD08	A^2 in		$4A^2$	$8A^6$	$16A^6$	$32A^{26}$
XnD09	A^3 in		$4A^3$	$8A^7$	$16A^7$	$32A^{27}$
XnD10	A^4 in	$1C$				
XnD11		$1D$				
XnD12		$1E$				
XnD13	B^4 out	$1F$				
XnD14	B^3 out		$4C^0$	$8B^0$	$16A^8$	$32A^{28}$
XnD15	B^2 out		$4C^1$	$8B^1$	$16A^9$	$32A^{29}$
XnD16	B^1 out		$4D^0$	$8B^2$	$16A^{10}$	
XnD17	B^0 out		$4D^1$	$8B^3$	$16A^{11}$	
XnD18	B^0 in		$4D^2$	$8B^4$	$16A^{12}$	
XnD19	B^1 in		$4D^3$	$8B^5$	$16A^{13}$	
XnD20	B^2 in		$4C^2$	$8B^6$	$16A^{14}$	$32A^{30}$
XnD21	B^3 in		$4C^3$	$8B^7$	$16A^{15}$	$32A^{31}$
XnD22	B^4 in	$1G$				
XnD23		$1H$				
XnD24		$1I$				
XnD25		$1J$				
XnD26			$4E^0$	$8C^0$	$16B^0$	
XnD27			$4E^1$	$8C^1$	$16B^1$	
XnD28			$4F^0$	$8C^2$	$16B^2$	
XnD29			$4F^1$	$8C^3$	$16B^3$	
XnD30			$4F^2$	$8C^4$	$16B^4$	
XnD31			$4F^3$	$8C^5$	$16B^5$	
XnD32			$4E^2$	$8C^6$	$16B^6$	
XnD33			$4E^3$	$8C^7$	$16B^7$	
XnD34		$1K$				
XnD35		$1L$				
XnD36		$1M$		$8D^0$	$16B^8$	
XnD37		$1N$		$8D^1$	$16B^9$	
XnD38		$1O$		$8D^2$	$16B^{10}$	
XnD39		$1P$		$8D^3$	$16B^{11}$	
XnD40				$8D^4$	$16B^{12}$	
XnD41				$8D^5$	$16B^{13}$	
XnD42				$8D^6$	$16B^{14}$	
XnD43				$8D^7$	$16B^{15}$	
XnD49	C^4 out					$32A^0$
XnD50	C^3 out					$32A^1$
XnD51	C^2 out					$32A^2$
XnD52	C^1 out					$32A^3$
XnD53	C^0 out					$32A^4$
XnD54	C^0 in					$32A^5$
XnD55	C^1 in					$32A^6$
XnD56	C^2 in					$32A^7$
XnD57	C^3 in					$32A^8$
XnD58	C^4 in					$32A^9$
XnD61	D^4 out					$32A^{10}$
XnD62	D^3 out					$32A^{11}$
XnD63	D^2 out					$32A^{12}$
XnD64	D^1 out					$32A^{13}$
XnD65	D^0 out					$32A^{14}$
XnD66	D^0 in					$32A^{15}$
XnD67	D^1 in					$32A^{16}$
XnD68	D^2 in					$32A^{17}$
XnD69	D^3 in					$32A^{18}$
XnD70	D^4 in					$32A^{19}$