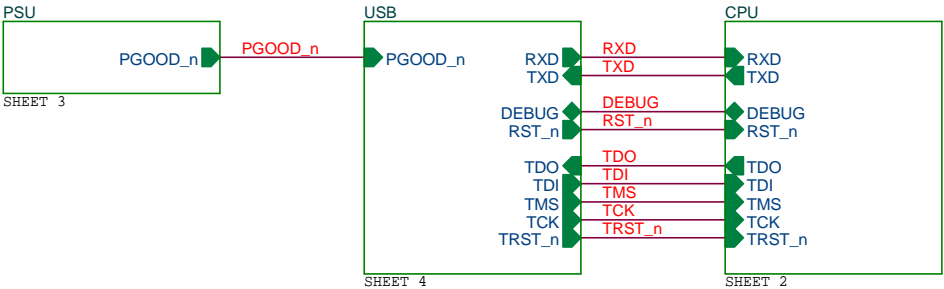
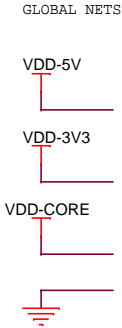


XC-5: XS1-L1-64TQFP DEVELOPMENT XCARD




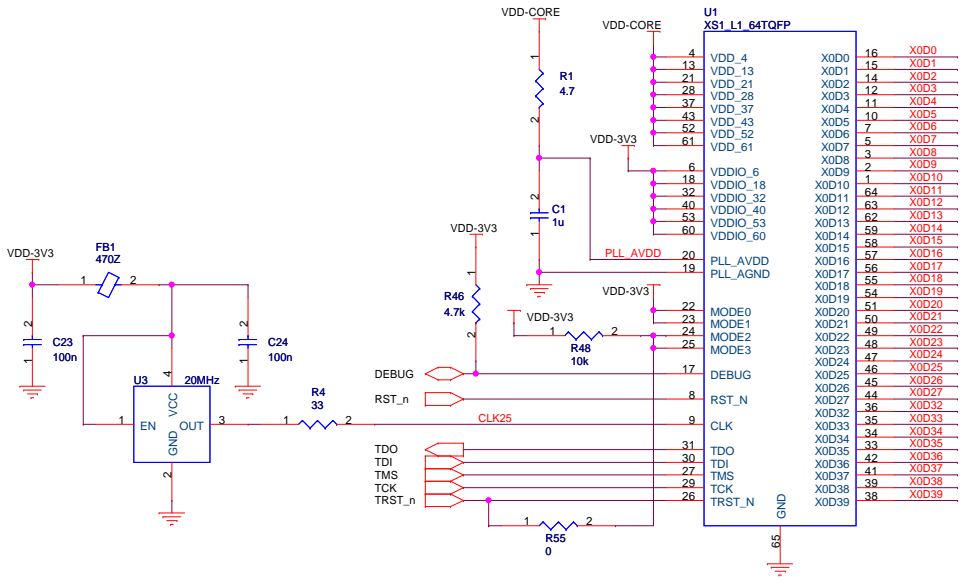
ALLEGRO CONSTRAINT NOTES

		MIN	MAX	
PCS	DEFAULT	0.15	0.15	
	PCS_CLK	0.15	0.15	
	PCS_PWR	0.3		
	PCS_DP	TBD	TBD	IMPEDANCE DEPENDANT
SCS	DEFAULT	0.15		
	SCS_CLK	0.3		
	SCS_DP	0.3		
ECS	ECS_SHORT			



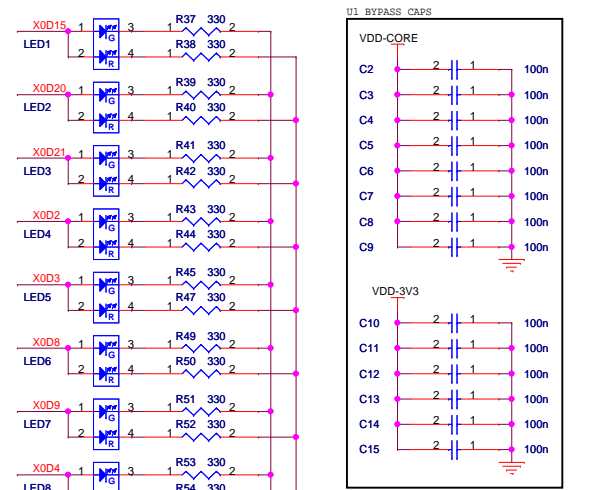
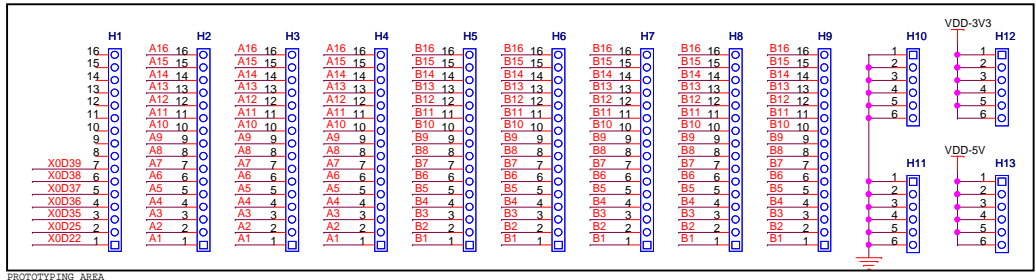
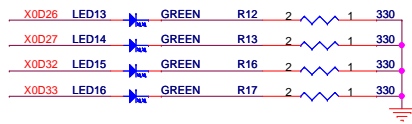
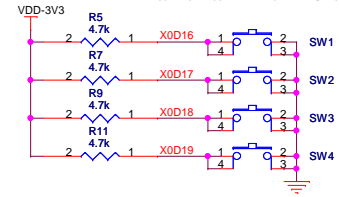
AN1  PCB XC-5 REV 1.0

Schematic: ROOT		 ©COPYRIGHT 2009 http://www.varisys.co.uk
Title: XMOS XC-5		
Rev: 1.0	Date: Friday, July 03, 2009	
Sheet 1 of 4	Document No.: <Doc>	

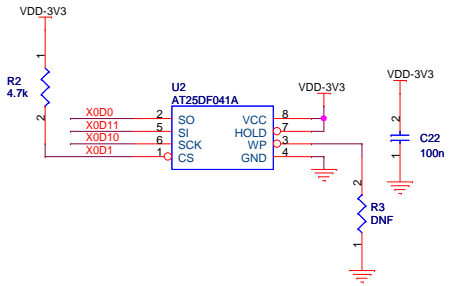
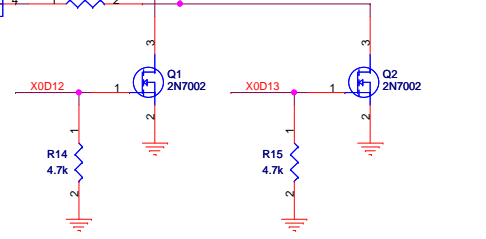


PORT ASSIGNMENTS									
1b	4b	8b	16b	SIGNAL					
P1A0				SPI MISO					
P1B0				SPI SS					
P4A0	P8A0	P16A0		USER LED 1					
P4A1	P8A1	P16A1		USER LED 2					
P4B0	P8A2	P16A2		USER LED 3					
P4B1	P8A3	P16A3		USER LED 4					
P4B2	P8A4	P16A4		USER LED 5					
P4B3	P8A5	P16A5		USER LED 6					
P4A2	P8A6	P16A6		USER LED 7					
P4A3	P8A7	P16A7		USER LED 8					
P1C0				SPI CLK					
P1D0				SPI MOSI					
P1E0				USER LED GREEN SELECT					
P1F0				USER LED RED SELECT					
P4C0	P8B0	P16A8		USER LED 9					
P4D0	P8B2	P16A10		KEY 1					
P4D1	P8B3	P16A11		KEY 2					
P4D2	P8B4	P16A12		KEY 3					
P4D3	P8B5	P16A13		KEY 4					
P4C2	P8B6	P16A14		USER LED 11					
P4C3	P8B7	P16A15		USER LED 12					
P1G0				PROTOTYPE AREA					
P1H0				UART TX (XS1 TO HOST)					
P1I0				UART RX (HOST TO XS1)					
P1J0				PROTOTYPE AREA					
P4E0				KEY LED 1 / PROTOTYPE AREA					
P4E1				KEY LED 2 / PROTOTYPE AREA					
P4E2				KEY LED 3 / PROTOTYPE AREA					
P4E3				KEY LED 4 / PROTOTYPE AREA					
P1K0				SPARE / PROTOTYPE AREA					
P1L0				PROTOTYPE AREA					
P1M0				PROTOTYPE AREA					
P1N0				PROTOTYPE AREA					
P1O0				PROTOTYPE AREA					
P1P0				PROTOTYPE AREA					

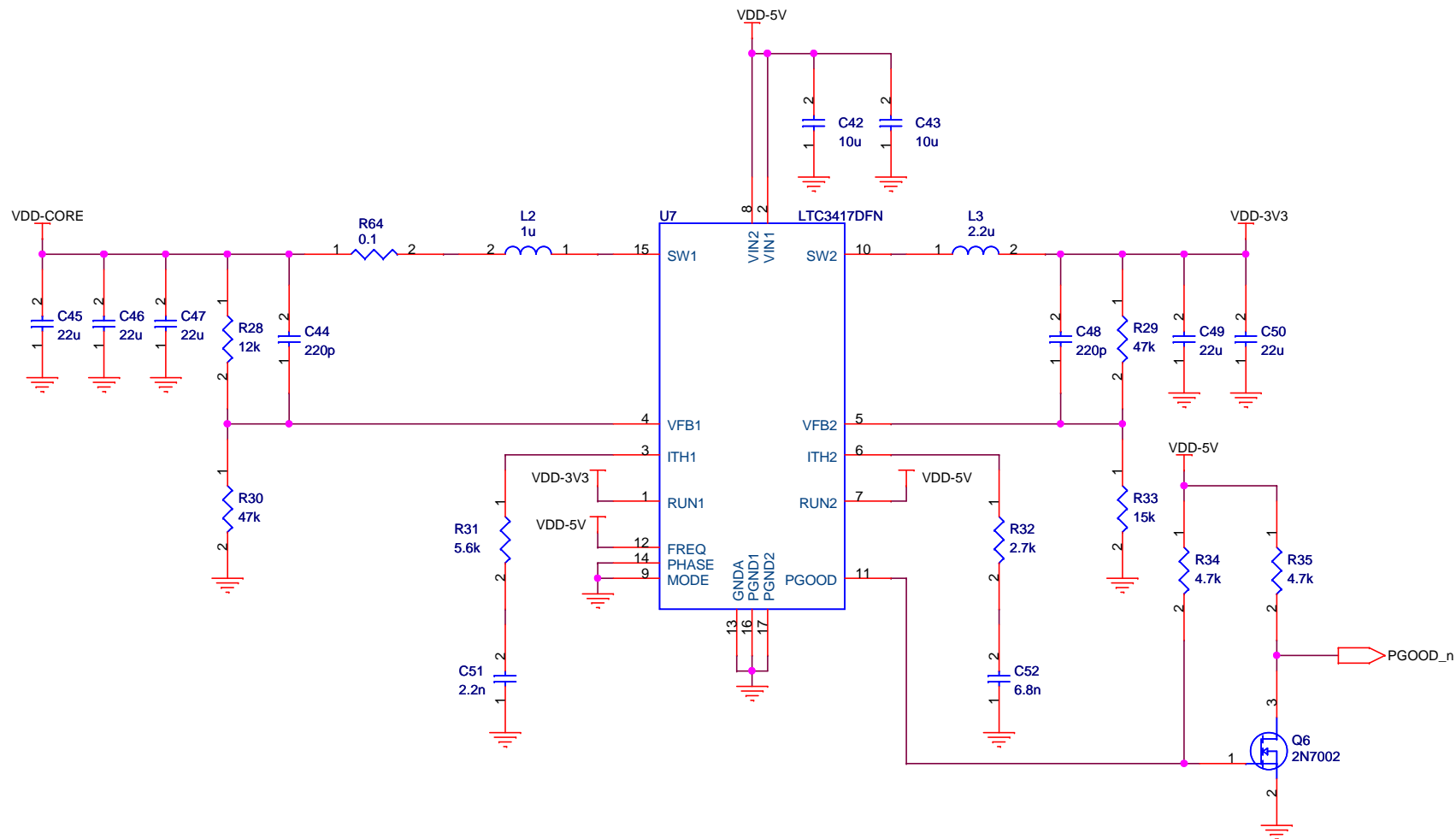
NOTE: THESE SWITCHES HAVE A SLIGHTLY INCORRECT FOOTPRINT FOR THE SPECIFIED EPH




NOTE: RED and GREEN LEDs are reversed due to footprint error.



Schematic: CPU	
Title: XMOS XC-5	
Rev: 1.0	Date: Friday, July 03, 2009
Sheet 2 of 4	Document No.: <Doc>



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