U16 sliceKIT Core Board Hardware Manual

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XMOS

SYNOPSIS

This document pertains to the 1V3 revision of the U16 sliceKIT Core Board.

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1 Overview

IN THIS CHAPTER

1.1 Introduction

This document covers the hardware design of the sliceKIT U16 Core Board, USB sliceCARDs and Mixed Signal sliceCARD.

The Core Board contains a fully pinned out 16-core xCORE-USB Processor, with its GPIOs connected to two expansion connectors (termed `Slots`) to interface with expansion cards called sliceCARDs which plug into the slots. The Core Board has two further specialist `Slots`, one for USB connectivity and one providing access to the on chip ADC available on the xCORE device. The Core Board also contains all circuitry necessary for operating and debugging the XMOS system. Multiple sliceKIT Core Boards can be interconnected to form a multi XMOS device system with dual 5-bit XMOS Links being present between the boards. The U16 Core Board is only capable of being the start of a chain i.e. the chain master.

1.2 sliceKIT System Layout

The diagram below shows an overview of the layout of the U16 Core Board with sliceCARDs attached. Each of the four slots has a specific label - `Diamond`, `Square`, `USB` (labelled U) and `Mixed Signal` (labelled A), printed on the U16 Core Board silkscreen. The `Diamond` Slice slot contains 24 xCORE IOs and the `Square` Slice slot 20 xCORE IOs (usable as GPIO or two 5-wire XMOS links). The `Mixed Signal` Slice slot contains 8 xCORE IOs along with 8 ADC channels, and the `USB` Slice slot contains 8 xCORE IOs along with the USB differential data signals. The label denotes which sliceCARDs are compatible with which Core Board Slots. The sliceCARDs are also marked with one or more of these labels to identify the slot type(s) they function correctly with.

All Slots are 36 pin PCI express style connectors in either socket or edge finger (plug) types.

`Diamond` and `Square` Slots are pinned out from Tile 1 of the U16 xCORE and the `USB` (U) and `Mixed Signal` (A) Slots from Tile 0.

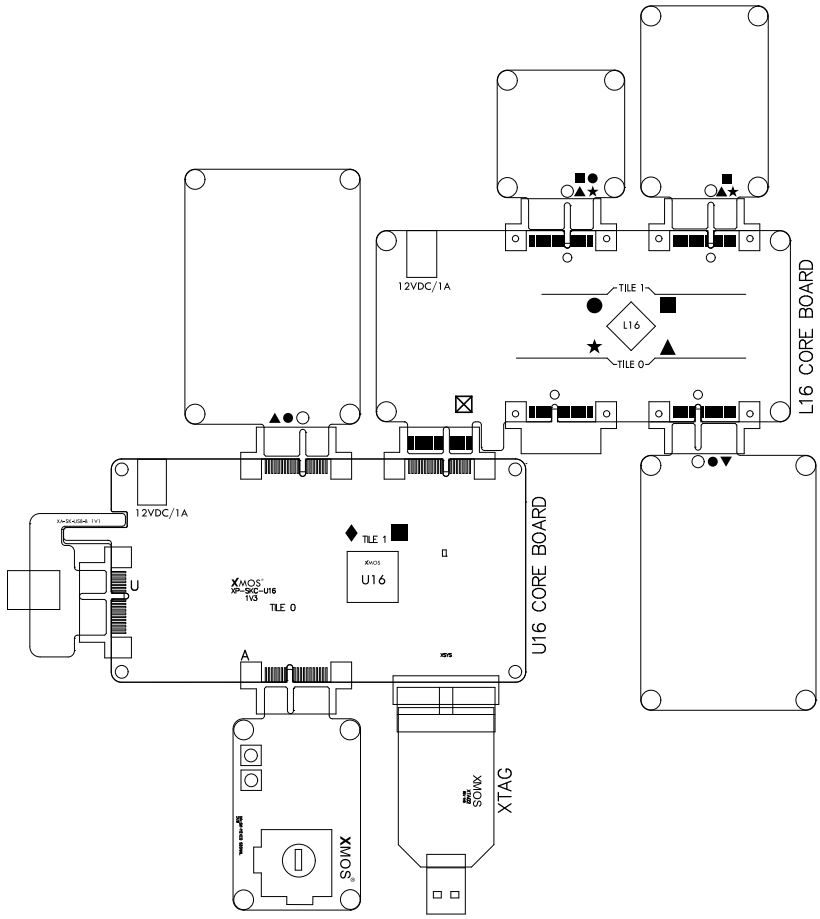

Figure 1: sliceKIT system diagram

2 Core Board

IN THIS CHAPTER

The Core Board contains the XMOS device plus support circuitry.

A single XS1-U16A-128 device has all of its GPIO connected to the Slots.

2.1 Multiple Core Boards

Additional L2 and A16 sliceKIT Core Boards can be connected to the first board's `Square` slot via the second board's `Chain` Slot to add extra processing capability and I/O through extra sliceCARDs. The first such board is termed the Master, the remaining boards as Slaves. When there is only one board, it is the Master.

2.2 Setup

The Core Board is powered by a 12V external power supply.

For debugging, an XSYS connector is available on the Core Board to allow connection of an xTAG to provide a debug link from a USB host.

2.3 Power Supply

Power input to the sliceKIT Core Board is via a standard barrel jack connector. A standard 12V external power supply should be used to power the board. Each Core Board requires its own 12V supply. This input supply is used to generate the main 5V board supply via a DC-DC converter.

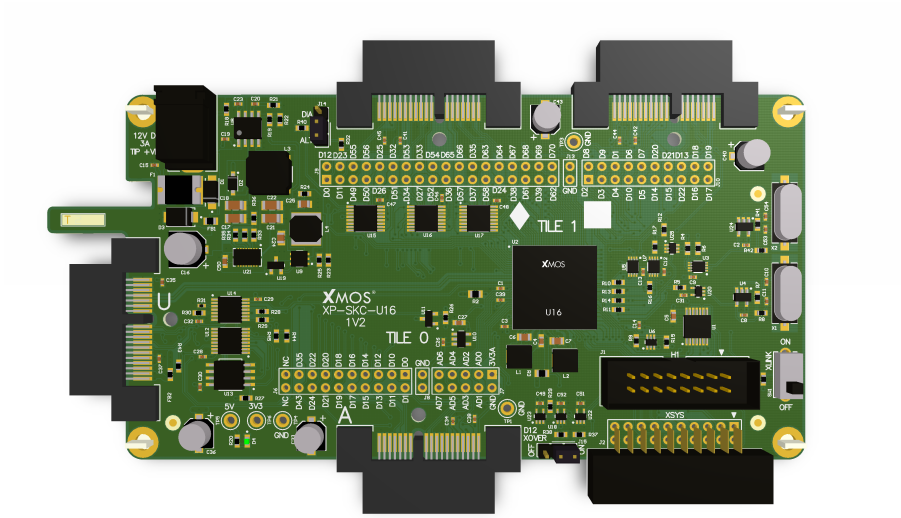

Figure 2: U16 sliceKIT Core Board

The 5V board supply is then fed to all the Slot connectors as well as powering the Core Board itself. A 3V3 I/O supply is generated by a DC-DC converter from the 5V main supply, and a 3V3 analogue supply is generated by an LDO converter from the 5V main supply.

The Core Board provides 3V3 and 5V at 0.25A to each slot for a total of approximately 2W per slice.

2.4 Debug

Debug of the system is via the XSYS Connector.

The JTAG signals are connected as shown below.

A presence detect signal is present on both the `Square` Slot connector to allow detection of a connected board and subsequent automatic switching of the JTAG chain. In a system of multiple Core Boards, the Master is the source of the JTAG chain so the system can only be debugged from the master. Other boards will see no devices in the JTAG chain.

The use of xSCOPE is covered in the XMOS Links section (2.6). The xSCOPE xCONNECT link can be either enabled or disabled via a switch on the Core Board labelled `XLINK`.

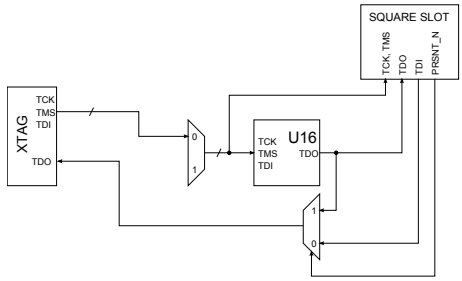

Figure 3: JTAG Chain

2.5 U16 Boot

Master Core Boards boot from SPI flash, while slave Core Boards boot from xCONNECT link `XLB` from the next connected Core Board.

To allow re-use of the SPI boot pins (ports 1A, 1B, 1C, 1D) as signal I/O pins for the `USB` and `Mixed Signal` slot, a latched bus switch is used which connects the xCORE SPI pins to either the SPI Flash or to the sliceCARD Slots. The switch is controlled by X0D14 and X0D15. Once the device has booted X0D14 is used to enable or disable the SPI interface, X0D15 should then transition from low to high to latch the selection. The SPI selection state is then maintained until the system is reset.

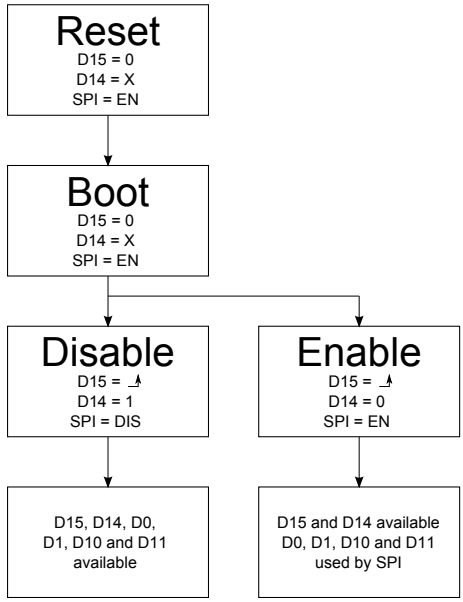

Figure 4: SPI Select Flow Diagram

Once this sequence is completed the selection has been latched therefore X0D14 and X0D15 return to performing their normal functions in the USB slot.

If the SPI is not disabled, then sliceCARDs in the USB and Mixed Signal slots may not function as expected. If there are no sliceCARDs in the USB or Mixed Signal slots, then it does not matter whether the SPI has been disabled or not. Therefore, applications which require runtime access to the SPI flash should either leave the USB and Mixed Signal slots unpopulated or check to ensure that the Card(s) which are in there will be unaffected by the operation of the Flash.

The XTAG2 system can use the boot mode select signal to force all devices in the chain (master and slave Core Boards) to boot from JTAG (don't boot) for debug purposes.

If not in this mode, the devices will boot from SPI or xCONNECT link as appropriate.

2.6 XMOS Links

The Square slot contains two 5-bit XMOS Links, XLA and XLB, which can be used for chaining sliceKIT Core Boards together.

It is recommended that if a sliceCARD that requires the use of the 4-bit port (X0D16-19) is used in the Mixed Signal Slot the xSCOPE switch is off on the Core Board to ensure correct operation of the sliceCARD in the Mixed Signal slot. This is due to the 4-bit port being shared with the xSCOPE xCONNECT link.

2.7 Reset

The whole system is held in reset until all power supplies are stable, and reset is connected to all sliceCARDs so any circuitry on them can be reset. It also indicates to the sliceCARDs that their power input is stable. The reset from the XTAG2 resets the whole system, if required for debugging.

2.8 Clocking

There are two clock sources available on the Core Board. One provides a 25MHz system clock, the other is a 24MHz clock provided to the U16 device.

The system clock from a Master Core Board is fed automatically to all of the slave Core Boards so the whole system will operate synchronously.

The system clock is also fed to each of the sliceCARD slots.

2.9 Testpoints

Each xCORE I/O signal is also available on a 0.1" header, next to the Slot that it is connected to. These connections can be used to connect an oscilloscope or logic analyzer, or for interconnection of signals for advanced development work.

The signals are identified on the silkscreen layer of the sliceKIT Core Board, the table below lists their relationship to the internal ports.

U16 Pin	Slot	PCIE	Function				
X0D0	USB	A7	P1A0				
X0D1	MIXED SIG	B15	P1B0				
X0D10	MIXED SIG	B2	P1C0				
X0D11	USB	A8	P1D0				
X0D12	USB	A9	P1E0				
X0D13	MIXED SIG	A3	P1F0				
X0D14	USB	B7		P4C0	P8B0	P16A8	P32A28
X0D15	USB	B8		P4C1	P8B1	P16A9	P32A29
X0D16	MIXED SIG	B13		P4D0	P8B2	P16A10	
X0D17	MIXED SIG	B14		P4D1	P8B3	P16A11	
X0D18	MIXED SIG	A4		P4D2	P8B4	P16A12	
X0D19	MIXED SIG	A12		P4D3	P8B5	P16A13	
X0D20	USB	B10		P4C2	P8B6	P16A14	P32A30
X0D21	USB	B11		P4C3	P8B7	P16A15	P32A31
X0D22	MIXED SIG	B4	P1G0				
X0D24	NA	NA	P1I0				
X0D35	USB	A10	P1L0				
X0D43	NA	NA			P8D7	P16B15	
X1D0	DIAMOND	B2	P1A0				
X1D1	SQUARE	A8	P1B0				
X1D2	SQUARE	B6		P4A0	P8A0	P16A0	P32A20
X1D3	SQUARE	B7		P4A1	P8A1	P16A1	P32A21
X1D4	SQUARE	B9		P4B0	P8A2	P16A2	P32A22
X1D5	SQUARE	B11		P4B1	P8A3	P16A3	P32A23
X1D6	SQUARE	A9		P4B2	P8A4	P16A4	P32A24
X1D7	SQUARE	A11		P4B3	P8A5	P16A5	P32A25
X1D8	SQUARE	A6		P4A2	P8A6	P16A6	P32A26
X1D9	SQUARE	A7		P4A3	P8A7	P16A7	P32A27
X1D10	SQUARE	B10	P1C0				
X1D11	DIAMOND	B4	P1D0				
X1D12	DIAMOND	A3	P1E0				
X1D13	SQUARE	A15	P1F0				
X1D14	SQUARE	B12		P4C0	P8B0	P16A8	P32A28
X1D15	SQUARE	B13		P4C1	P8B1	P16A9	P32A29
X1D16	SQUARE	B17		P4D0	P8B2	P16A10	
X1D17	SQUARE	B18		P4D1	P8B3	P16A11	
X1D18	SQUARE	A17		P4D2	P8B4	P16A12	
X1D19	SQUARE	A18		P4D3	P8B5	P16A13	
X1D20	SQUARE	A12		P4C2	P8B6	P16A14	P32A30

(continued)

U16 Pin	Slot		PCIE	Function			
X1D21	SQUARE	A13		P4C3	P8B7	P16A15	P32A31
X1D22	SQUARE	B15	P1G0				
X1D23	DIAMOND	A4	P1H0				
X1D24	DIAMOND	B15	P1I0				
X1D25	DIAMOND	A8	P1J0				
X1D26	ALT DIAMOND	B9		P4E0	P8C0	P16B0	
X1D27	ALT DIAMOND	B11		P4E1	P8C1	P16B1	
X1D32	ALT DIAMOND	A9		P4E2	P8C6	P16B6	
X1D33	ALT DIAMOND	A11		P4E3	P8C7	P16B7	
X1D34	DIAMOND	B10	P1K0				
X1D35	DIAMOND	A15	P1L0				
X1D36	ALT DIAMOND	B12	P1M0		P8D0	P16B8	
X1D37	ALT DIAMOND	B13	P1N0		P8D1	P16B9	
X1D38	ALT DIAMOND	B17	P1O0		P8D2	P16B10	
X1D39	ALT DIAMOND	B18	P1P0		P8D3	P16B11	
X1D49	DIAMOND	B6					P32A0
X1D50	DIAMOND	B7					P32A1
X1D51	ALT DIAMOND	A6					P32A2
X1D52	ALT DIAMOND	A7					P32A3
X1D53	DIAMOND	A9					P32A4
X1D54	DIAMOND	A11					P32A5
X1D55	DIAMOND	A6					P32A6
X1D56	DIAMOND	A7					P32A7
X1D57	DIAMOND	B12					P32A8
X1D58	DIAMOND	B13					P32A9
X1D61	DIAMOND	B17					P32A10
X1D62	DIAMOND	B18					P32A11
X1D63	DIAMOND	A17					P32A12
X1D64	DIAMOND	A18					P32A13
X1D65	DIAMOND	A12					P32A14
X1D66	DIAMOND	A13					P32A15
X1D67	NA	NA					P32A16
X1D68	NA	NA					P32A17
X1D69	NA	NA					P32A18
X1D70	NA	NA					P32A19

2.10 Loop-back Port

Jumper J15 can be used to enable a loop-back between a 1-bit port on each of the two tiles. With the loop-back enabled port X0D13 is connected to X1D12, and

disconnected from the Mixed Signal slot. With the loop-back disabled X0D13 is connected to the Mixed Signal slot.

2.11 Diamond/Alt Diamond Slot

The I/Os connected to the Diamond slot can be changed to an alternative configuration known as Alt Diamond, this is controlled by setting the jumper J14.

The Diamond configuration exposes 16 bits of the 32-bit port, which can be useful for applications requiring a wide bus, the Alt Diamond configuration exposes more 1-bit ports.

2.12 Slot Pinouts

The signal assignments for the connectors on the Core Board and sliceCARDs can be seen in the table below.

2.12.1 USB

PCIE B (TOP)	SIGNAL	FUNCTION
B1	VBUS IN	VBUS FROM USB CONNECTOR
B2	VBUS IN	VBUS FROM USB CONNECTOR
B3	*GND*	POWER SUPPLY GROUND
B4	VBUS OUT	VBUS TO USB CONNECTOR
B5	VBUS OUT	VBUS TO USB CONNECTOR
B6	*GND*	POWER SUPPLY GROUND
B7	X0D14	P4C0 P8B0 P16A8 P32A28
B8	X0D15	P4C1 P8B1 P16A9 P32A29
B9	*GND*	POWER SUPPLY GROUND
B10	X0D20	P4C2 P8B2 P16A10
B11	X0D21	P4C3 P8B3 P16A11
KEY	**KEY**	**MECHANICAL KEY**
B12	*GND*	POWER SUPPLY GROUND
B13	*GND*	POWER SUPPLY GROUND
B14	USB DP	USB DATA POSITIVE
B15	USB DN	USB DATA NEGATIVE
B16	*GND*	POWER SUPPLY GROUND
B17	*GND*	POWER SUPPLY GROUND
B18	*GND*	POWER SUPPLY GROUND

PCIE A (BOT)	SIGNAL	FUNCTION
A1	VBUS IN	VBUS FROM USB CONNECTOR
A2	VBUS IN	VBUS FROM USB CONNECTOR
A3	*GND*	POWER SUPPLY GROUND
A4	VBUS OUT	VBUS TO USB CONNECTOR
A5	VBUS OUT	VBUS TO USB CONNECTOR
A6	*GND*	POWER SUPPLY GROUND
A7	X0D0	P1A0
A8	X0D11	P1D0
A9	X0D12	P1E0
A10	X0D35	P1L0
A11	NC	NOT CONNECTED
KEY	**KEY**	**MECHANICAL KEY**
A12	*GND*	POWER SUPPLY GROUND
A13	*GND*	POWER SUPPLY GROUND
A14	*GND*	POWER SUPPLY GROUND
A15	*GND*	POWER SUPPLY GROUND
A16	*GND*	POWER SUPPLY GROUND
A17	NC	NOT CONNECTED
A18	*3V3*	3.3V POWER SUPPLY

2.12.2 MIXED SIGNAL

PCIE B (TOP)	SIGNAL	FUNCTION
B1	*3V3A*	ANALOG 3.3V POWER SUPPLY
B2	X0D10	P1C0
B3	*GND*	POWER SUPPLY GROUND
B4	X0D22	P1G0
B5	*3V3*	3.3V POWER SUPPLY
B6	ADC0	ADC CHANNEL 0
B7	ADC1	ADC CHANNEL 1
B8	*GND*	POWER SUPPLY GROUND
B9	*GND*	POWER SUPPLY GROUND
B10	ADC2	ADC CHANNEL 2
B11	ADC3	ADC CHANNEL 3
KEY	**KEY**	**MECHANICAL KEY**
B12	*GND*	POWER SUPPLY GROUND
B13	X0D16	P4D0 P8B2 P16A10
B14	X0D17	P4D1 P8B3 P16A11
B15	X0D1	P1B0
B16	*GND*	POWER SUPPLY GROUND
B17	*GND*	POWER SUPPLY GROUND
B18	NC	NOT CONNECTED

PCIE A (BOT)	SIGNAL	FUNCTION
A1	NC	NOT CONNECTED
A2	*5V*	POWER SUPPLY 5V
A3	X0D13	P1F0
A4	X0D18	P4D2 P8B4 P16A12
A5	*GND*	POWER SUPPLY GROUND
A6	ADC4	ADC CHANNEL 4
A7	ADC5	ADC CHANNEL 5
A8	*GND*	POWER SUPPLY GROUND
A9	ADC6	ADC CHANNEL 6
A10	*GND*	POWER SUPPLY GROUND
A11	*GND*	POWER SUPPLY GROUND
KEY	**KEY**	**MECHANICAL KEY**
A12	X0D19	P4D3 P8B5 P16A13
A13	NC	NOT CONNECTED
A14	*GND*	POWER SUPPLY GROUND
A15	NC	NOT CONNECTED
A16	*RST_N*	SYSTEM RESET (ACTIVE LOW)
A17	ADC7	ADC CHANNEL 7
A18	*GND*	POWER SUPPLY GROUND

2.12.3 SQUARE

PCIE B (TOP)	SIGNAL	FUNCTION				
B1	*DEBUG*	XSYS DEBUG SIGNAL				
B2	*TCK*	XSYS TCK SIGNAL				
B3	*GND*	POWER SUPPLY GROUND				
B4	*TDI*	XSYS TDI SIGNAL				
B5	*3V3*	POWER SUPPLY 3.3V				
B6	X1D2		P4A0	P8A0	P16A0	P32A20
B7	X1D3		P4A1	P8A1	P16A1	P32A21
B8	*GND*	POWER SUPPLY GROUND				
B9	X1D4		P4B0	P8A2	P16A2	P32A22
B10	X1D10	P1C0				
B11	X1D5		P4B1	P8A3	P16A3	P32A23
KEY	**KEY**	**MECHANICAL KEY**				
B12	X1D14		P4C0	P8B0	P16A8	P32A28
B13	X1D15		P4C1	P8B1	P16A9	P32A29
B14	*CLK*	MAIN SYSTEM CLOCK				
B15	X1D22	P1G0				
B16	*GND*	POWER SUPPLY GROUND				
B17	X1D16		P4D0	P8B2	P16A10	
B18	X1D17		P4D1	P8B3	P16A11	

PCIE A (BOT)	SIGNAL	FUNCTION
A1	*MSEL*	XSYS MSEL SIGNAL
A2	*5V*	POWER SUPPLY 5V
A3	*TMS*	XSYS TMS SIGNAL
A4	*TDO*	XSYS TDO SIGNAL
A5	*PRSNT*	SYSTEM PRESENT SIGNAL (ACTIVE LOW)
A6	X1D8	P4A2 P8A6 P16A6 P32A26
A7	X1D9	P4A3 P8A7 P16A7 P32A27
A8	X1D1	P1B0
A9	X1D6	P4B2 P8A4 P16A4 P32A24
A10	*GND*	POWER SUPPLY GROUND
A11	X1D7	P4B3 P8A5 P16A5 P32A25
KEY	**KEY**	**MECHANICAL KEY**
A12	X1D20	P4C2 P8B6 P16A14 P32A30
A13	X1D21	P4C3 P8B7 P16A15 P32A31
A14	*GND*	POWER SUPPLY GROUND
A15	X1D13	P1F0
A16	*RST_N*	SYSTEM RESET (ACTIVE LOW)
A17	X1D18	P4D2 P8B4 P16A12
A18	X1D19	P4D3 P8B5 P16A13

2.12.4 DIAMOND

PCIE B (TOP)	SIGNAL	FUNCTION
B1	NC	NOT CONNECTED
B2	X1D0	P1A0
B3	*GND*	POWER SUPPLY GROUND
B4	X1D11	P1D0
B5	*3V3*	POWER SUPPLY 3.3V
B6	X1D49	P32A0
B7	X1D50	P32A1
B8	*GND*	POWER SUPPLY GROUND
B9	X1D51	P32A2
B10	X1D34	P1K0
B11	X1D52	P32A3
KEY	**KEY**	**MECHANICAL KEY**
B12	X0D57	P32A8
B13	X1D58	P32A9
B14	*CLK*	MAIN SYSTEM CLOCK
B15	X1D24	P1I0
B16	*GND*	POWER SUPPLY GROUND
B17	X1D61	P32A10
B18	X1D62	P32A11

PCIE A (BOT)	SIGNAL	FUNCTION
A1	NC	NOT CONNECTED
A2	*5V*	POWER SUPPLY 5V
A3	X1D12	P1E0
A4	X1D23	P1H0
A5	*GND*	POWER SUPPLY GROUND
A6	X1D55	P32A6
A7	X1D51	P32A7
A8	X1D25	P1J0
A9	X1D53	P32A4
A10	*GND*	POWER SUPPLY GROUND
A11	X1D54	P32A5
KEY	**KEY**	**MECHANICAL KEY**
A12	X1D65	P32A14
A13	X1D66	P32A15
A14	*GND*	POWER SUPPLY GROUND
A15	X1D35	P1L0
A16	*RST_N*	SYSTEM RESET (ACTIVE LOW)
A17	X1D63	P32A12
A18	X1D64	P32A13

2.12.5 ALT DIAMOND

PCIE B (TOP)	SIGNAL	FUNCTION				
B1	NC	NOT CONNECTED				
B2	X1D0	P1A0				
B3	*GND*	POWER SUPPLY GROUND				
B4	X1D11	P1D0				
B5	*3V3*	POWER SUPPLY 3.3V				
B6	X1D49					P32A0
B7	X1D50					P32A1
B8	*GND*	POWER SUPPLY GROUND				
B9	X1D26		P4E0	P8C0	P16B0	
B10	X1D34	P1K0				
B11	X1D27		P4E1	P8C1	P16B1	
KEY	**KEY**	**MECHANICAL KEY**				
B12	X0D36	P1M0		P8D0	P16B8	
B13	X1D37	P1N0		P8D1	P16B9	
B14	*CLK*	MAIN SYSTEM CLOCK				
B15	X1D24	P1I0				
B16	*GND*	POWER SUPPLY GROUND				
B17	X1D38	P1O0		P8D2	P16B10	
B18	X1D39	P1P0		P8D3	P16B11	

PCIE A (BOT)	SIGNAL	FUNCTION	
A1	NC	NOT CONNECTED	
A2	*5V*	POWER SUPPLY 5V	
A3	X1D12	P1E0	
A4	X1D23	P1H0	
A5	*GND*	POWER SUPPLY GROUND	
A6	X1D51		P32A7
A7	X1D52		P32A8
A8	X1D25	P1J0	
A9	X1D32	P4E2 P8C6 P16B6	
A10	*GND*	POWER SUPPLY GROUND	
A11	X1D33	P4E3 P8C7 P16B7	
KEY	**KEY**	**MECHANICAL KEY**	
A12	X1D65		P32A14
A13	X1D66		P32A15
A14	*GND*	POWER SUPPLY GROUND	
A15	X1D35	P1L0	
A16	*RST_N*	SYSTEM RESET (ACTIVE LOW)	
A17	X1D63		P32A12
A18	X1D64		P32A13

2.12.6 System Services Slot Signals

On all Slots, TDO is always out of the sliceKIT Core Board, TDI is always in to the Core Board.

MSEL, TCK, TMS, RST_N are all inputs to the Core Board from the XSYS Connector and outputs from the Core Board on the `Square` Slot.

DEBUG is bidirectional.

PRSNT_N is used on the `Square` Slot to detect another Core Board is connected. This signal is used to switch the JTAG chain signals.

CLK and RST_N are output from all Slots.

3 USB sliceCARDs

IN THIS CHAPTER

USB sliceCARDs connect to the PCI-E 36 pin connector J4 on the U16 Core Board. They have a unique key design in order to prevent them being plugged in to non USB slice slots and prevent non USB slices being plugged in to a USB slice slot. The detail for the key design and the PCI-E 36 card edge finger can be seen in the figure below:

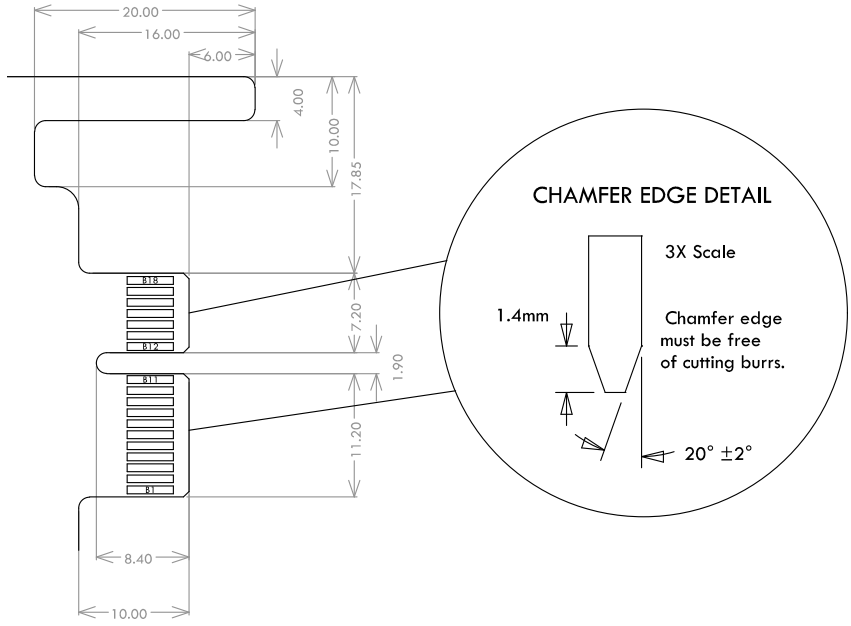

Figure 5: USB Slice Detail

3.1 U16 USB Slice Pinout

The table below details the pinout of the USB slice connector from the U16 Core Board:

PCIE B (TOP)	SIGNAL	FUNCTION	PCIE A (BOT)	SIGNAL	FUNCTION
B1	VBUS IN	VBUS FROM USB HOST	A1	VBUS IN	VBUS FROM USB HOST
B2	VBUS IN	VBUS FROM USB HOST	A2	VBUS IN	VBUS FROM USB HOST
B3	*GND*	POWER SUPPLY GROUND	A3	*GND*	POWER SUPPLY GROUND
B4	VBUS OUT	VBUS TO USB DEVICE	A4	VBUS OUT	VBUS TO USB DEVICE
B5	VBUS OUT	VBUS TO USB DEVICE	A5	VBUS OUT	VBUS TO USB DEVICE
B6	*GND*	POWER SUPPLY GROUND	A6	*GND*	POWER SUPPLY GROUND
B7	X0D14	USB SEL 1	A7	X0D0	RESERVED
B8	X0D15	USB SEL 2	A8	NC	NOT CONNECTED
B9	*GND*	POWER SUPPLY GROUND	A9	X0D11	I2C SCL
B10	X0D20	RESERVED FOR MFI	A10	X0D35	I2C SDA
B11	X0D21	RESERVED FOR MFI	A11	NC	NOT CONNECTED
KEY	**KEY**	**MECHANICAL KEY**	**KEY**	**KEY**	**MECHANICAL KEY**
B12	*GND*	POWER SUPPLY GROUND	A12	*GND*	POWER SUPPLY GROUND
B13	*GND*	POWER SUPPLY GROUND	A13	*GND*	POWER SUPPLY GROUND
B14	USB DP	USB DATA POSITIVE	A14	*GND*	POWER SUPPLY GROUND
B15	USB DN	USB DATA NEGATIVE	A15	*GND*	POWER SUPPLY GROUND
B16	*GND*	POWER SUPPLY GROUND	A16	*GND*	POWER SUPPLY GROUND
B17	*GND*	POWER SUPPLY GROUND	A17	NC	NOT CONNECTED
B18	*GND*	POWER SUPPLY GROUND	A18	*3V3*	3.3V POWER SUPPLY

Figure 6: USB Slice Pinout

3.2 USB AB Slice

The USB AB slice consists of a USB A connector, USB B connector and a high-speed 2:1 switch to select between them.

By default the USB data signals from the B type connector are routed to the U8 device on the U16 board. When the USB B connector is being routed the LED next to the connector is illuminated. In order to route the USB data signals from the A type connector the *USB_SEL* line should be bought high. When the USB A connector is being routed the LED next to the connector is illuminated.

5V is supplied to the USB A connector to provide VBUS to connected devices.

The figure below shows the layout of the USB A/B slice:

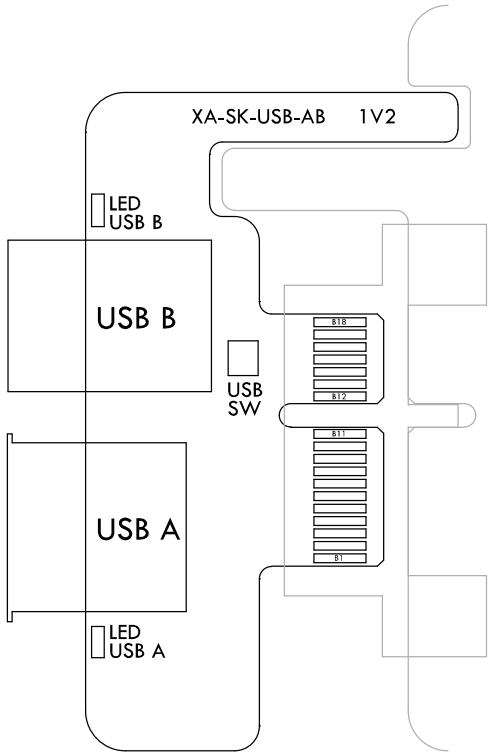

Figure 7: USB AB Slice

4 New Designs Based on sliceKIT

IN THIS CHAPTER

There are a number of sections of the design of the sliceKIT platform that have been optimized for flexibility to cover as many use cases as possible. Therefore some consideration may be required in what to leave out or change in a custom design. Some of the important points to consider are dealt with in this section.

Some general points to consider when implementing your own design are:

- Always check the datasheet of the xCORE device. In the case where the reference design and datasheet conflict, the datasheet presides.
- XMOS datasheets contain additional hardware design requirements and guidelines that are not covered in this document, which users of XMOS hardware reference designs must ensure are followed.
- The presence of a third party device in an XMOS hardware reference design does not make any statement about its general availability. You must make your own arrangements to ensure that all components can be sourced in the required volumes.

4.1 USB

The U16 sliceKIT platform has been designed to allow for a number of options when it comes to USB connectivity. In a custom design it is highly unlikely that a high-speed connector will be required, hence the USB slice connector can be removed and your own connectivity option can be implemented.

For all USB implementations the following points should be considered:

- Keep USB data lines as short as possible
- The USB data differential pair should have a characteristic impedance of 90R
- Common mode chokes, vias, connectors and stubs should be avoided if at all possible to maximise signal integrity

- For further information refer to High Speed USB Platform Design Guidelines[1]

The U16 Core Board USB design is a compromise to allow for maximum flexibility in use. Therefore it should not be used as a reference for custom designs that require full USB compliance.

4.1.1 USB Device (B)

For a simple device only configuration a USB B connector (standard, mini or micro size) should be connected directly to the USB data lines of the U16 device. If the device is to be bus powered an ESD device can be added to clamp the data lines to VBUS and ground and the connection to the U16 VBUS pin can be omitted. If the device is to be self powered then the data lines should only be clamped to ground, and the VBUS input should be connected to the U16 VBUS pin to detect host connection.

4.1.2 USB Host (A)

To implement a host only connection a USB A connector should be directly connected to the USB data lines of the U16 device. The VBUS power supply will need to be provided locally. An ESD device can be added to clamp the data lines to VBUS and ground.

4.1.3 Multi Mode USB

For more complex configurations requiring a number of host and/or device connections to be available one or more high speed capable USB bus switches can be used, with the routing being controlled using one of the wider ports available on the U8 device. There are many options for deciding which port to route to (and consequently which code to boot) from a user input switch to sensing connections and deciding priority.

4.2 Power Supply

Depending on the configuration required the local power supply may need to be able to supply VBUS to a device, as well as supporting self and/or bus powered modes.

4.2.1 Bus Powered Device

For a purely USB bus powered device the external power supply DC-DC supply and preferential 5V and over current limit device can be omitted.

Some form of VBUS to 3.3V converter will be required to supply VDDIO, and a second supply will be required for the on chip ADC if it is to be used.

[1] http://www.usb.org/developers/docs/hs_usb_pdg_r1_0.pdf

4.2.2 Self Powered Device

For a purely self powered device the preferential 5V and over current device can be omitted. Some sort of external power supply will be required to generate rails suitable for the U16 VSUP supply (5V or 3.3V), the U16 VDDIO supply (3.3V) from an external supply.

A second 3.3V supply will be required for the on chip ADC if it is to be used.

If a lower power suspend mode is required a power supply with an enable function, or some sort of high side switch circuit may be necessary.

4.2.3 Bus or Self Powered Device

For systems designed to operate either bus or self powered some sort of external power supply will be required to generate 5V for the U16 VSUP supply when the system is self powered.

The preferential 5V device (or similar supply selection device) will be required. Note that a simple diode OR, using Schottky diodes is not suitable as the reverse current leakage leads to the voltage on the VBUS sense pin rising above the threshold leading to inaccurate detection of the presence of a host, which in turn can lead to issues enumerating on the USB.

Some form of VBUS to 3.3V converter will be required to supply VDDIO, and a second supply will be required for the on chip ADC if it is to be used.

If a lower power suspend mode is required a power supply with an enable function, or some sort of high side switch circuit will be necessary.

4.2.4 Self Powered Host

For a self powered host the preferential 5V device can be omitted, but the rest of the power supply sections need to be present in some form. An over-current switch should be added and set accordingly to comply with the USB specification.

The design of the external power supply should be customized to your own requirements, however a 5.5V over-voltage trip circuit should be implemented to protect the device on the USB, and remain within the USB specification.

The external power supply will be required to generate rails suitable for the U16 VSUP supply (5V or 3.3V), the U16 VDDIO supply (3.3V).

A second 3.3V supply will be required for the on chip ADC if it is to be used.

4.3 Portmap

Due to the flexibility of the I/O on an xCORE device the location of the signals routed to the U16 can be easily optimized for your own layout.

As a general rule any 1-bit port pin can be easily swapped with any other. The only fixed 1-bit port pins are those connected to the SPI bus of the code flash device.

The location of signals on the 4-bit ports can be swapped with other signals on the same port, and the ports as a whole can be swapped, however care should be taken to ensure that all signals on the same port should be in the same direction i.e. all outputs or all inputs.

The 32-bit port on the MFA board is used as an output port, hence all signals on this port are output only.

4.4 SPI Routing Control

In order to maximize the functionality of the MFA platform all of the 1-bit ports used by the boot flash can also used by the system after boot. In order to allow for this the SPI 1-bit ports are latched to either the flash device or to the I/O.

If your design does not make use of all of the 1-bit ports then the slave select line should be left to only control the SPI interface and the rest of the SPI 1-bit ports can be reused.

4.5 Debug Interface

During the development phase of a new design it is highly recommended that the full XSYS debug interface, including the xSCOPE xCONNECT link, should be included. This allows for full programming and debug interfaces.

Once the design is stable the xSCOPE xCONNECT link can be omitted, and if space is a concern the main JTAG signals can be bought out to a custom header, or test points.

For high volume builds it is possible to omit the debug interface altogether, however this will require another method of programming the flash e.g. preprogrammed before placement.

For single device designs most of the switching and buffering devices for the JTAG chain can be omitted.

4.6 Device Clock

It should be noted that if an external clock signal is used the maximum signal level should be 1.8V. The output from the 1.8V DCDC regulator on the device can be used to provide an appropriate supply (VDD1V8 pins).

This does not apply if a crystal is used to provide a clock to the device as the clock signal is generated internally from the 1.8V supply.

5 Errata

IN THIS CHAPTER

5.1 1V2 Hardware SPI Bus Switch

On revision 1V2 hardware the SPI bus switch enable/disable line is connected to X0D16 (rather than X0D14 as stated above). This signal is shared with the xSCOPE xCONNECT link which means that xSCOPE can not be used if control of the SPI bus is required.