MFA platform (XK-USB-AUDIO-U8-2C) - Clock Design Advisory

IN THIS DOCUMENT

- Introduction
- Solution

1 Introduction

An error has been discovered in the MFA hardware platform (XK-USB-AUDIO-U8-2C) revision 1V1. The source of the system clock from the PLL device is 3.3V, however the XS1-U8A-64 device requires a clock with a nominal voltage of 1.8V. Providing a 3.3V clock will not prevent a device from working, but it is likely to reduce the life of the xCORE device.

This error has been remedied on the 1V2 revision of the hardware.

2 Solution

Care should be taken to ensure the clock signal on designs based on the MFA platform do not exceed 1.8V. There are three options to ensure this is the case:

1. Use a crystal instead of an external clock. If a crystal is used it should be 12MHz or 24MHz and have appropriate padding capacitors.

2. Reduce the signal level of the external clock using a buffer IC that can run from a 1.8V supply while remaining 3.3V tolerant. The 1.8V supply may be taken from VDD1V8 on the XS1-U8A-64 device (pin M4).

3. Reduce the signal level of the external clock using a resistor divider. Care should be taken with the resistor values to ensure the RC value, taking the internal capacitance of the XI pin, allows for an appropriate signal level, while keeping the DC path to ground sufficiently high. The values of the resistors will also be reliant on the drive strength of the clock source. With the PLL on the MFA board, the values 390R and 430R have been found to be appropriate.

Option 1 is preferable, but if an external 3.3V clock source is to be used, it is recommended that option 2 be considered first. Option 3 should only be used where option 2 is not appropriate.

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